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Technical Report -80-E-4

AN AIRBORNE PROGRAMMABLE DIGITAL TO VIDEO CONVERTER INTERFACE AND OPERATION MANUAL.

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USAAV

FEBRUARY 1981

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SCAN CONVERTER
VIDEO DISPLAY
TELEVISION DISPLAY

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the operational commands, data structure and storage, and interface to an airborne programmable digital to video converter. It is intended for use as a companion manual to the hardware description report No. AVRADCOM TR 80-E-5.

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INTERFACE AND OPERATION MANUAL

INTRODUCTION

This report describes the operational commands, data structure and storage, and interface to the Airborne Programmable Digital To Video Converter (DVC), which is shown in Figure 1. It is intended for use as a companion manual to the hardware description report entitled An Airborne Programmable Digital To Video Converter, Technical Report No. AVRADCOM TR 80-E-5.

The DVC accepts and converts data from an external digital computer into a standard 525 line television format which can be displayed either in black and white or color. The system was developed for night navigation/pilotage and nap-of-the-earth helicopter flight studies.

Survivability of Army helicopters under the threat of radar-directed anti-aircraft weapons requires flying at or below tree top level during day and night conditions. The pilot must be aware of the upcoming terrain characteristics. At present, low level operations are performed with the pilot dedicated to the task of piloting the vehicle. The copilot verbally informs the pilot of upcoming terrain from hand-held maps. At night, this is extremely difficult. Improving the method of informing the pilot of approaching terrain, thus reducing the hazards of low level night flight, are the desired goals of this project.

The design goal was to develop a general purpose computer-driven display whose information content and control functions could be determined by software. Contour maps displaying up to 16 shades of grey or color and various aircraft symbology were the two main items to be displayed.

DESCRIPTION OF DISPLAY SYSTEM

Figure 2 is a block diagram of the Airborne Display System showing the location and functional interface of the Digital to Video Converter. The display system is under control of a Singer Kearfott SKC 2000 computer. The computer generates the map data base based upon the selected operation program and the aircraft sensor inputs. A typewriter terminal is used as an interface with the system operator for control and status information. Map and alphanumeric data are entered into the converter via the SKC Computer Bus consisting of a 32-line data bus, a 16-line address bus, and a 9-line control bus. The computer can also read data from the converter along with the converter status information. Under computer control, the converter will display the map and alphanumeric data on any combination of the three television monitors shown. Synchronization signals are also supplied to the monitors as well as the other external video sources. The converter will also display or mix with the map data video from up to four external sources such as a television camera or symbology generation equipment upon control from the computer.

DIGITAL TO VIDEO CONVERTER REQUIREMENTS

The converter is required to perform the following as part of an integrated display system:

1. Be programmable from an external Singer Kearfott SKC 2000 computer system in both data format and control function selection.

2. Provide output data which are compatible with a standard 525-line interlaced raster scan television format and operate with either 512 by 512 or 256 by 256 pixel/line resolutions.

3. Provide storage and operational capability for the display of maps in 16 shades-of-grey or 8 color hues, with superimposed flight symbols, and alphanumeric characters.

4. The display memory must be available to the Singer Kearfott computer for use as a stand alone auxiliary read/write memory when not in use for display purposes.

5. Provide, under software control, synchronization to external video sources, mix external and internal video signals, and be synchronized from external synchronization sources.

6. Output data selection under software control for display on two black and white television monitors and/or a three gun color television monitor.

7. Be packaged in an approved airborne enclosure and be capable of being flight tested in a helicopter.

DESCRIPTION OF THE DIGITAL TO VIDEO CONVERTER

Figure 3 is a simplified block diagram of the DVC. The SKC Computer Bus consisting of 32 data lines, 16 address lines, and 9 control lines, interfaces the converter with the host computer. The control lines consist of handshake and operational mode signals for controlling the flow of data between the two units. These lines are routed to the Central Processing Unit (CPU) which controls the overall operation of the converter. The CPU contains an 8085 microprocessor to permit versatile programmable operation of the converter. The CPU communicates with the rest of the converter via its own CPU Bus consisting of a data, address, and control structure. A memory for the CPU is located on the CPU Bus and contains the software and data storage for operation of the converter. The data and address lines from the SKC Computer are routed to the SKC Data and Address Interface where they can be connected to the Input Bus data and address lines respectively under control of the CPU. In the proper mode, the SKC Computer can read or write from the Display Memories which are also connected to the Input Bus in the converter. This permits the computer to load map, alphanumeric, and symbology data into the Display Memories for future display or utilize these memories for bulk RAM storage. Five Display Memories are available in the converter. Each memory contains 8K 32-bit words which is sufficient storage capacity to store one bit level of a 512 pixel/line by 525-line per frame raster scan television display. Four of these memories are used to store the map data, thus permitting a 16 shades-of-grey map presentation on a conventional black and white interlaced television monitor. The fifth Display Memory is used for the storage of alphanumeric or flight symbol data which is only displayed in a black and white format. This data can be entered from the computer or can be locally generated by the converter CPU. The Input Bus Memory Controller provides two functions. The first is to generate the necessary timing and interface signals for the Display Memories when they are accessed by either the SKC Computer or CPU via the Input Bus. The second is to provide an 8-bit to 32-bit data bus interface along with an address interface to permit the CPU to access the Display Memories. The Display Memories also have an additional port to the Display Bus. The Display Bus is primarily used by the Map Generator to read data from the Display Memories for display. The CPU determines the bus, Input or Display, to which each of the five individual Display Memories is connected. Thus, it is possible to have some of the Display Memories utilized for display while the balance of the memories are being accessed by the SKC Computer or CPU for the loading of new data. The Display Bus Memory Controller functions in a similar fashion to the Input Bus Controller except that it provides timing, data, and address access functions for the CPU and Map Generator for access of Display Memories via the Display Bus. The Map Generator reads data from the Display Memories, formats the data, and provides the necessary timing signals for the display of maps and symbology on a television monitor. The Map Generator contains a programmable cathode ray tube (CRT) controller which is accessed by the CPU to permit operation in a wide variety of modes. The Alphanumeric Generator permits the converter to display alphanumeric messages on the television monitors. These messages can be generated by the CPU or entered from the SKC Computer to the Display Memories where they are accessed by the CPU for display via the Alphanumeric Generator. The output from the Alphanumeric and Map Generators are fed to the Video Mixer for transmission to two black and white television monitors for display. The Video Mixer is also under program control of the CPU for selection of the converter output video and optional mixing of the converter video with up to four external video signals. The output of the Map Generator is also fed to the Color Generator which converts the map and symbology data into red, blue, and green color monitor drive signals for optional display in color. The Sync Distribution circuitry provides standard television synchronization signals for use internal to the converter and distribution to external equipment. This circuitry under CPU control can also receive sync signals from an external source for subsequent synchronization of the converter and distribution to external equipment. The Power Supply provides all necessary operating potentials for the converter circuitry.

INTERFACE

The interface to the DVC is described in two parts. The first part concerns the interface to the host Singer Kearfott Computer over which data and control commands are transferred. The second part describes the electrical characteristics of the various input/output (I/O) ports of the DVC.

a. To The Singer Kearfott Computer (SKC) 1

(1) Hardware Description

A block diagram of the SKC Computer/DVC Interface is given in Figure 4. Electrical connection is made via plug 17J1 on the front panel of the DVC, Figure 1. There are nine twisted pair control signals between the host SKC Computer and the DVC to permit the computer to direct and monitor the operation of the DVC. Differential line drivers and receivers are used on each control line pair to provide high noise immunity. The 9614 line driver and 9615 line receiver manufactured by Fairchild are used for these functions respectively and operate at standard TTL logic levels. A three state 32-line data bus, DBUSSKC/, is used to transfer data on a bidirectional basis between the computer and the DVC. The data on the bus has a negative true polarity and utilizes DS7835 bus transceivers manufactured by National Semiconductor which operate at standard TTL logic levels. A unidirectional 16 line address bus, ABUSSKC/, permits the computer to specify the location in the DVC Display Memory for the desired memory access. The address on the bus has a negative true polarity and the DS7835 bus transceivers used on this bus are connected for operation in a unidirectional manner.

This description covers the DVC interface when the CPU board is installed. The DVC interface for use when the Temporary CPU board is installed is described in Appendix A.

(2) Functional Operation

The function of each SKC-DVC interface signal is described below. Throughout the description, SKC will refer to the SKC Computer and DVC will refer to the Digital to Video Converter.

Controls Signals

Mnemonic	Description
MCLRSKC	Master Clear from the SKC, clears all circuitry in the DVC logic 1 performs a master clear logic 0 indicates no master clear
MCRSKC	Memory Cycle Request from the SKC, indicates the SKC is requesting an access of the DVC Display Memory logic 1 indicates a cycle request logic 0 indicates no cycle request
MCACK	Memory Cycle Acknowledge from the DVC, indicates to the SKC that a requested access of the Display Memory is in progress logic 1 indicates a cycle acknowledge logic 0 indicates no cycle acknowledge

The MCACK goes to a 1 upon the beginning of the memory cycle request service and is terminated by MCC

MCC Memory Cycle Complete from the DVC, indicates to the SKC that a requested access of the Display Memory is complete

logic 1 indicates completion of the memory cycle
logic 0 indicates the memory cycle is in progress

The MCC is a pulse of approximately 200 ns in length

DPSKC Data Processed from the SKC, indicates to the DVC that the data from the DVC has been accepted by the SKC after a Display Memory read cycle is complete.

logic 1 indicates the data has been accepted the SKC
logic 0 indicates the data is being processed

The DPSKC is a pulse of approximately 500 ns in length

WRITSKC Memory Write Command from the SKC, determines if the Display Memory cycle requested is in the read or write mode

logic 1 indicates a memory write cycle
logic 0 indicates a memory read cycle

OMREQ Operational Mode Request from the SKC, indicates that the SKC is requesting a change in the operational mode of the DVC. This signal sets an interrupt request to the DVC CPU which will be serviced by the CPU when the present operating routine can be interrupted. The CPU will then fetch and execute the instruction specified by the Control Words stored in Display Memory 1 by the SKC.

logic 1 indicates a OMREQ is present
logic 0 indicates the OMREQ is off

OMACK Operational Mode Acknowledge from the DVC, indicates to the SKC that an OMREQ has been received and is being serviced

logic 1 indicates the OMACK is present
logic 0 indicates the OMACK is off

The OMACK will go to a 1 while the OMREQ is being serviced and return to 0 upon completion of service.

DMARDY Direct Memory Access (DMA) ready from the DVC, indicates to the SKC that the DVC is ready for a DMA operation. The DVC must presently be instructed to enter the DMA mode via a Control Word from the SKC. The DMARDY indicates to the SKC when the DMA set-up is complete.

logic 1 indicates the DMARDY is present
logic 0 indicates the DMARDY is off

Data Bus

DBUSSKC/ A 32-line bidrectional bus used for the transfer of data between the SKC and the DVC. The polarity of data on the bus is negative true.

Address Bus

ABUSSKC/ A 16-line unidirectional bus from the SKC to the DVC which is used specify the Display Memory location for an access request. The polarity of the address on the bus in negative true.

b. Input/Output (I/O) Characteristics

All I/O connections to the DVC are made from the front panel, Figure 1. The synchronization outputs, Horizontal Drive, Vertical Drive, and Composite Sync each have five outputs for driving external equipment at the standard EIA voltage output levels. The external synchronization inputs provide the capability to synchronize the DVC from an external source. There are two voltage levels for these inputs, TTL positive true levels for horizontal and vertical drive, and standard EIA levels for horizontal drive vertical drive and composite sync. The external sync inputs are selectable under software control form the host SKC Computer as described in Appendix C. There are four external video inputs which are also selectable under software control (see Operation Section and Appendix C) from the SKC Computer for mixing with the DVC video. There are also video outputs for the black and white (B/W) monitors 1 & 2 and the three color drive signals for a color monitor. All video I/O signals operate at standard 0- to 1-volt video levels. The prime power consisting of 28 VDC at 5 amperes for the DVC circuitry and 120 volts AC at 400 Hz for the cooling fans enters through receptacle 17J6. A ground connection and six test points are provided to monitor the major internal power supply voltages for diagnostic purposes.

DATA STORAGE

a. Description

The organization of memory within the DVC is shown in Table 1. The address locations 0000H to 5800H are reserved for the CPU within the DVC and are not accessible by the SKC Computer. This data field width is 8 bits (1 byte). The address locations 0000H to 57FFH contain 22k bytes of ultraviolet erasable programmable read only memory (EPROM) which contain the DVC system operating program for the CPU. This portion of the memory utilizes 2716 EPROM integrated circuits which must be externally programmed from appropriate EPROM programming equipment. The addresses 5800H to 5BFFH contain 1k bytes of random access memory (RAM) for use by the CPU for the temporary storage of operational data and computations. This section of the memory utilizes 2114 static RAM integrated circuits. The next block of memory, addresses 5C00H to 5FFFH, contain 1k bytes of RAM utilized for the Alphanumeric Page Memory. The page memory can only be written into by the DVC CPU and is used to store the alphanumeric message presently being displayed. This section of memory utilizes 2114 static RAM integrated circuits. The five Display Memories comprise addresses 6000H through FFFFH. Each Display Memory contains 8k addresses and has a 32-bit (4 byte) data field width. These five memories are used to store both symbolic and shades-of-grey map data for display and are accessible from both the CPU and SKC Computer. These memories utilize 2108 dynamic RAM integrated circuits.

b. Display Memories

Data is written or read from the Display Memories by the SKC Computer via the 32-line data bus (DBUSSKC/) at the location specified on the 16 line address bus (ABUSSKC/) from the SKC Computer as shown in Figure 3. The address allocation for each Display Memory is shown in Table 1. Upon command from the SKC Computer, the DVC CPU can also access the Display Memories via the Input Bus Memory Controller. In the Display Mode, the Display Memories are utilized for display purposes and can not be accessed by the SKC Computer. Upon display, each data word is shifted out of the respective memory in a serial fashion such that bit 1 is accessed first and bit 32 last. Display Memory 1 is used to store black and white (B/W) data such as flight symbols, contour lines, or alphanumeric characters generated by an external source. The converter can be externally programmed (see Operation Section and Appendix C) to inset onto the display background either a white or a black trace when a logical "1" is read from this memory. The white and the black intensity levels are set by hardware internal to the DVC. Data from Display Memories 2-5 contains the map shades-of-grey information and is routed to addresses A0 - A3 respectively of the Map Video PROM. Thus, Display Memory 2 is the least significant bit and Display Memory 5 is the most significant bit of the map display brightness. The additional PROM addresses A4 - A7, which are supplied by the CPU, determine the mapping mode of the DVC which is described in more detail in Operation Section and Appendices B and C.

(1) Map Data Storage Format for 512 Pixels/Line Resolution

In the 512 pixels/line operating mode, raster scanning is performed in an interlaced pattern. Field 0 is the even field. During scanning of this field, 240 even numbered scan lines, No 0, 2, 4, to 478 respectively are displayed. During the alternate odd field, Field 1, the 240 odd numbered scan lines, No 1, 3, 5, to 479 respectively are displayed. Figure 5 is the map display format showing the order and location of the displayed memory words. The Display Memory allocation for Field 0 is shown in Table 2, and the allocation for Field 1 in Table 3. The odd field is the first displayed field upon initialization of the display.

(2) Map Data Storage Format for 256 Pixels/Line Resolution

In the 256 pixels/line operating mode, identical display data is presented for both the first displayed field, Field 0, and again for the alternate field, Field 1. Figure 6 is the map display format showing the order and location of the displayed memory words on a field basis. The Display Memory allocation for this mode of operation is shown in Table 4.

(3) Alphanumeric Message Storage

In addition to the storage of map data, each of the five Display Memories contains a storage allocation for two alphanumeric messages for a total of 10 messages. These messages each have the 64 characters/line, 15-line display format of Figure 7 and are called a Lower Alphanumeric Message and an Upper Alphanumeric Message respectively. These messages are intended to be used for labeling or prompting purposes by the host SKC Computer. The source data for these messages is written into the Display Memories by the SKC Computer in the same 4-byte word format and manner as the map data. The storage allocation for these messages in the Display Memories is shown in Table 5. Addresses M000H to NDFFH are utilized for map data storage only. The next 240 words, addresses NE00H to NEEFH, contain the Lower Alphanumeric Message and the Upper Alphanumeric Message is located at addresses NF00H through NFEFH in each Display Memory. The data format for each SKC Computer word in the alphanumeric message is shown in Figure 8. Each word is divided into four bytes. Each byte specifies one alphanumeric character, hence, each SKC Computer word specifies four (4) alphanumeric characters. The lowest order character is specified by byte 0 and the highest order character by byte 3. Upon Control Word command (see Appendix C, either Display, Modify Alphanumeric Data) from the SKC Computer, a message can be selected by the DVC CPU and written into the Alphanumeric Page Memory for display. The messages in the Display Memories may also be selectively cleared by utilizing the Memory Preset/Clear Control Word from the SKC Computer.

c. CPU Memory Allocation

The CPU memory allocation contains a total of 24k bytes of memory. The field width is one byte/word. The CPU memory allocation is contained in addresses 0000H to 5FFFH as shown in the DVC Memory organization of Table 1. A further breakdown of the CPU memory is given in the CPU/Alphanumeric Page Memory organization of Table 6. There is 6k bytes of EPROM memory available at addresses 0000H to 1FFFH for storage of the DVC System Operating Program for the CPU. The EPROM memory consists of three (3) 2716 EPROMs which are manufactured by Intel and are located in sockets on the CPU memory board. The 2716s must be externally programmed on a suitable microprocessor development system. The 16k bytes of memory, addresses 2000H to 57FFH, are not used at this time but can be hardwired at a future time to accommodate a combination of EPROM and RAM memory. There is 1k bytes of static RAM memory at addresses 5800H to 5BFFH which is available for temporary storage by the CPU during the execution of the System Operating Program.

d. Alphanumeric Page Memory Organization and Display Format

The Alphanumeric Page memory organization is shown in the lower portion of Table 6. The 960 bytes of RAM memory at addresses 5C00H to 5FBFH are locations of the Alphanumeric Page. The data field width is one byte/word. The 64 addresses at 5FC0H to 5FFFH are also part of the Alphanumeric Page but are not displayed. The displayed location of each data line and character is shown in the Alphanumeric Page display format of Figure 8. The expanded Alphanumeric Page memory map with the memory location of each data line and character is given in Table 7. Each byte of the page stores one (1) alphanumeric character for display and has the data format shown in Figure 9. Note that bit 7 of each byte contains the character generator ROM select code. An 0 specifies the MCM6571AL Shifted ASCII Characters and Greek ROM, and a 1 specified the MCM6574L Math Symbols and Pictures ROM. Data bits 0-6 correspond to ROM addresses A0-A6 respectively. Both ROMs are manufactured by Motorola and the display pattern tables for each are given in Tables 8 & 9 respectively. The alphanumeric character dot matrix display format is given in Figure 10.

CONTROL WORDS

Four Control Words are used to direct the operation of the DVC from the host SKC Computer. The desired Control Word(s) are four bytes in width and are written into a non displayed section of Display Memory 1 by the SKC Computer when the Display Memories are made available to the computer for updating. There are two storage locations for the Control Words:

Address No	Memory Location
0	7FF0H
1	7FF1H

When a single Control Word operation is requested by the computer, the Control Word must be written into memory location 7FF0H. For operations requiring two Control Words such as Display, Control Word 0 is written into location 7FF0H and Control Word 1 is written into location 7FF1H. A brief discussion of each Control Word is given below. A detailed operational description of each Control Word is given in Appendix C.

Control Words 0 & 1, Display Function

These two words set the DVC operational status in the display mode. They control the map, B/W symbology, and alphanumeric page display functions along with the external video mixer.

Control Word 2, Memory Preset/Clear

This word presets/clears all or segments of the DVC memory.

Control Word 3, Modify Alphanumeric Data

This word reads a selected message from the Display Memory and writes the message into the Alphanumeric Page Memory.

OPERATION

a. Initialization

1. Prior to DVC power turn-on, all control lines should be placed in the logic 0 state to prevent the DVC from inadvertently performing an uninstructed operation after initialization.

2. Turn power on to the DVC, 28 VDC and 120 VAC 400 Hz.

3. Clear the DVC by setting MCLRSKC to a logic 1 and return to a logic 0 or push the MANCLR button located on the front panel of the DVC. The DVC will clear all circuitry and perform an initialization routine. After the initialization, all DVC Display Memories will be available to the SKC to accept data, and a OMACK will be sent to the SKC to indicate that the initialization is complete and the SKC may now enter data into the Display Memories.

b. RAM Memory Mode

The Display Memories in the DVC can be used as an auxiliary RAM memory of 40 k words (4 byte word length) for the SKC Computer when operated in the following manner:

Write Mode--To write data from the SKC into the DVC Display Memories:

1. Set WRITSKC to a logic 1
2. Place the data word on DBUSSKC/
3. Place the memory address on ABUSSKC/
4. Set the MCRSKC to a logic 1
5. The DVC will respond with a MCACK transition from a logic 0 to a logic 1 to acknowledge the memory cycle request. The SKC may now return MCRSKC to a logic 0.
6. The DVC will give a MCC transition from a logic 0 to a logic 1 to indicate when the memory cycle is complete. MCACK and MCC will then be returned to a logic 0.
7. The SKC can now write the next word into the DVC Display Memory.

Read Mode--To Read data from the DVC Display Memories to the SKC Computer:

1. Set WRITSKC to a logic 0
2. Place the desired address location on the address bus, ABUSSKC/
3. Set the MCRSKC to a logic 1
4. The DVC will respond with a MCACK transition from a logic 0 to a logic 1 to acknowledge the memory cycle request. The SKC may now return MCRSKC to a logic 0.
5. The DVC will give a MCC transition from a logic 0 to a logic 1 to indicate that the memory cycle is complete, and the memory data is on the data bus, DBUSSKC/. The MCACK will then be returned to a logic 0.
6. The DVC will hold the data on the DBUSSKC/ until a DPSKC is received from the SKC Computer to indicate that the data has been retained by the computer. Upon receipt of the DPSKC, the DVC will release the DBUSSKC/ and return MCC to a logic 0.

c. Display Mode

1. Initialize the DVC using the procedure of section a. above.
2. Load data from the SKC into the DVC Display Memories. This is done in following sequence:

(1) Set WRITSKC to a logic 1
(2) Place the data word on DBUSSKC/
(3) Place the memory address of ABUSSKC/
(4) Set the MCRSKC to a logic 1
(5) The DVC will respond with a MCACK transition from a logic 0 to a logic to acknowledge the memory cycle request. The SKC may now return MCRSKC to a logic 0.
(6) The DVC will give a MCC transition from a logic 0 to a logic 1 to indicate when the memory cycle is complete. MCACK and MCC will then be returned to a logic 0.
(7) The SKC can now write the next word into the DVC Display Memory.

3. Load data in the format of the two Display Control Words 0 & 1 into DVC Display Memory 1 at locations 7FF0H and 7FF1H respectively using the procedure of step 2. The functional format of these two Control Words is given in Appendix C.

4. Set OMREQ to a logic 1 to initiate the display turn-on. The DVC will turn-on the display in the mode specified by the Display Control Words and respond with a OMACK transition from a logic 0 to 1 when turn-on procedure has been completed. The SKC must then return OMREQ to a logic 0.

5. Set OMREQ to a logic 1 when it is desired for the DVC to leave the display mode. The DVC will extinguish the map display and leave on the alphanumeric and external video mixer functions as instructed in the Display Control Words 0 & 1, make all DVC Display Memories available to the SKC for updating, and respond with a OMACK transition from a logic 0 to 1. The SKC must then return OMREQ to a logic 0.

6. The SKC can then update the DVC Display Memories using the above steps 2-4.

d. DVC Memory Preset/Clear

1. When the Display Memories are available to the SKC for access, the SKC writes into memory location 7FF0H data to perform the desired memory preset/clear functions in accordance with the format of Control Word 2 of Appendix C.

2. Set the OMREQ to a logic 1 to initiate the memory preset/clear function. The DVC will respond with a OMACK transition from a logic 0 to a logic 1 when the task is finished. The SKC must then return OMREQ to a logic 0.

e. Modify Alphanumeric Data

1. When the Display Memories are available to the SKC for access, the SKC writes into memory location 7FF0H data to perform the desired modification of the alphanumeric data in accordance with the format of Control Word 3 of Appendix C.

2. Set the OMREQ to a logic 1 to initiate the modify alphanumeric data function. The DVC will respond with a OMACK transition from a logic 0 to a logic 1 when the task is finished. The SKC must then return OMREQ to a logic 0.

APPENDIX A

TEMPORARY CENTRAL PROCESSING UNIT (TCPU)

a. Introduction

The function of the TCPU is to provide an interface with the SKC Computer and a subset of control functions to permit limited operation of the DVC in the absence of the full microprocessor based CPU. The TCPU is intended to be utilized on a temporary basis until the full CPU is available. The TCPU will provide the following operational functions upon command from the SKC Computer:

(1) Initialization of the DVC to the following conditions:

1. Display of maps on monitor 1
2. Display of white contours or symbology on a black background on monitor 2
3. Synchronization set to internal
4. Resolution selectable from the SKC Computer to either 256 pixels/line or 512 pixels/line

(2) Display of maps in the following modes, selectable from the SKC Computer:

1. Eight (8) shades-of-grey (SOG) on a B/W monitor or eight color hues/intensities on a color monitor
2. Sixteen (16) SOG on a B/W monitor
3. A sliding grey scale consisting of an 8 SOG map presentation selected from the 16 SOG map data base

b. Hardware Description

A block diagram of the TCPU is shown in Figure A2. The TCPU contains a 4-bit counter which forms the lower four addresses of the data and address PROMs. The outputs of these PROMs are routed through bus drivers to the CPU Data Bus, DBUSCPU, and the CPU Address Bus, ABUSCPU, respectively. The higher order addresses for the PROMs are derived from the SKC computer interface based on the status of the control signals from the SKC. There is a divide by ten clock circuit which advances the counter and clocks the counter control logic. The counter control logic permits the TCPU to perform two functions, DVC initialization and setting of the map shades-of-grey display mode depending upon the logic level of the INIT/SHA signal from the SKC. In initialization mode, upon receipt of a trigger from the SKC, the counter advances through all 16 states which produces the necessary data, addresses from the PROMs and the I/O strobe, (I/O)/, to set the control registers in the DVC to perform in the desired display mode and turn-on of the display. In the shades-of-grey mode, the counter is advanced one state for each trigger received from the SKC which results in the data, address, and I/O strobe necessary to set the next shades-of-grey map display mode.

Clear circuitry is provided which permits the DVC to be cleared either by the SKC via MCLRSKC or manually through the MANCLR. There is also memory cycle logic to provide the interface signals between the SKC and the Display Memories in the DVC. The DISP/LOAD signal permits the Display Memories to be placed on the Display Bus for the display of maps and symbology or on the Input Bus for the accessing of the Display Memories from the SKC.

c. Interface to Singer Kearfott Computer (SKC)

The TCPU uses a modified interface which is shown in Figure A1. The control and bus signals use the same type of logic circuitry as the CPU interface which is described in the main body of the report. The function of each of the SKC-DVC interface signals is described below. Throughout the description, SKC will refer to the SKC Computer and DVC will refer to the Digital to Video Converter.

Control Signals

Mnemonic	Description
TRIGGER	TCPU operational trigger signal from the SKC. When the INIT/SHA signal is in the initialize mode (logic 1), the presence of a TRIGGER will initiate the initialization process. When the INIT/SHA signal is in the shades mode (logic 0), each trigger command will advance the TCPU circuitry to display maps in the next shades-of-grey display state as shown in Table A1. logic 0 to 1 transition performs the trigger operation
INIT/SHA	The initialize/shades signal from the SKC. A logic 1 places the TCPU in the initialize mode. A logic 0 places the TCPU in mode which determines the shades-of-grey display mode in accordance with Table A1.
RESOL	Resolution select from the SKC logic 0 selects 256 pixels/line logic 1 selects 512 pixels/line
SYMBRIT	Symbol brightness select from the SKC logic 0 selects black symbols logic 1 selects white symbols
MCLRSKC	Master Clear from the SKC, clears all circuitry in the DVC logic 1 performs a master clear logic 0 indicates no master clear

MCRSKC	Memory Cycle Request from the SKC, indicates the SKC is requesting an access of the DVC Display Memory logic 1 indicates a cycle request logic 0 indicates no cycle request
MCACK	Memory Cycle Acknowledge from the DVC, indicates to the SKC that a requested access of the Display Memory is in progress logic 1 indicates a cycle acknowledge logic 0 indicates no cycle acknowledge The MCACK goes to a 1 upon the beginning of the memory cycle request service and is terminated by MCC
MCC	Memory Cycle Complete from the DVC, indicates to the SKC that a requested access of the Display Memory is complete logic 1 indicates completion of the memory cycle logic 0 indicates the memory cycle is in progress The MCC is a pulse of approximately 200 ns in length
DPSKC	Data Processed from the SKC, indicates to the DVC that the data from the DVC has been accepted by the SKC after a Display Memory read cycle is complete logic 1 indicates the data has been accepted by the SKC logic 0 indicates the data is being processed The DPSKC is a pulse of approximately 500 ns in length
WRITSKC	Memory Write Command from the SKC, determines if the Display Memory cycle requested is in the read or write mode logic 1 indicates a memory write cycle logic 0 indicates a memory read cycle
DISP/LOAD	Display/Load control signal from the SKC logic 1 places all Display Memories in the display mode logic 0 places all Display Memories in a load mode in which the SKC can access these memories

Data Bus

DBUSSKC/	A 32 line bidirectional bus used for the transfer of data between the SKC and the DVC. The polarity of data on the bus is negative true.

Address Bus

ABUSSKC/ A 16 line unidirectional bus from the SKC to the DVC which is used specify the Display Memory location for an access request. The polarity of the address is negative true.

d. Digital to Video Converter Operation with the TCPU Board

The following sequence is to be used for the operation of the DVC from the SKC Computer when the TCPU board is used in place of the micro-processor based CPU board. The referenced mnemonics refer to the interface of section c above.

1. Prior to the turn-on of power to the DVC, the TRIGGER and MCREQSKC lines from the SKC should be set to logic 0. This is to prevent any inadvertent operation of the DVC after the reset is complete.

2. Turn primary power on to the DVC, 28 VDC and 120 VAC 400 Hz.

3. Clear the DVC Circuitry by setting MCLRSKC to a logic 1 and return to a logic 0, or by pushing the MANCLR button on the DVC front panel.

4. Set DISP/LOAD to a logic 0. This makes all 5 DVC Display Memories available to the SKC for the loading of display data.

5. Load data into the DVC Display Memories from the SKC Computer.

6. Set DISP/LOAD to a logic 1. This places all 5 DVC Display Memories in the display mode.

7. Set RESOL to determine the map display resolution:

   logic 1 for 512 pixels/line
   logic 0 for 256 pixels/line

8. Set INIT/SHA to a logic 1. This places the DVC in the initialization mode.

9. Give the TRIGGER a logic 0 to 1 transition and return to a logic 0. This initiates the initialization routine internal to the DVC.

10. Set INIT/SHA to a logic 0. This places the DVC in a mode to determine the map shades-of-grey (SOG) display presentation. To set the SOG mode, a counter internal to the DVC is advanced one state for each logic 0 to 1 transition of the TRIGGER line. The TRIGGER line should be returned to a logic 0 after each advancement of the counter. At least one TRIGGER command is required to turn the map display on. The state table for the

SOG operation is given in Table A1. An explanation of the map display modes and video truth table is given in Appendix B. If it is desired to change the SOG display mode while the display is in progress, the required number of TRIGGER commands can be given by the SKC to advance the SOG counter in the DVC to the desired map display state.

11. If the display does not come on in a satisfactory manner, clear the DVC with a MCLRSKC command or by pushing the MANCLR button, and repeat this operating routine starting at Step 8.

12. To stop the display, give the DVC a MCLRSKC command or push the MANCLR button. This will halt the display but will not alter the contents of the Display Memories in the DVC.

APPENDIX B

MAP VIDEO PROGRAMMABLE READ ONLY MEMORY (PROM)

The Map Video PROM (Figure B1) performs a digital mapping function between the four lines of input data and a four line video output. The mapping mode is determined by the state of the four control lines which are set by the CPU within the DVC. Various map display modes are available to the system operator who can select under software control the desired mode from the host SKC Computer. There are three basic modes of map display which are described in paragraphs a-c below. A truth table which describes each logic function is given in Table B1. Note that each operating mode contains the video output mapping function for all 16 states of the input data. Addresses A0 - A3 (data inputs) are connected to the data outputs from Display Memories 2 - 5 respectively. Addresses A4 - A7 (control lines) are the output bits 1 - 4 of the CPU Digital Display Register and are used to specify the mapping mode. The PROM outputs 00 - 03 drive the video digital to analog (D/A) converter within the DVC which provides the analog video output. 00 is the least significant converter bit and 03 is the most significant bit. A logic 1 on any of the four converter input lines corresponds to increasing the video output brightness.

a. Eight (8) Shades-of-Grey (SOG) Video

The mapping function for the eight SOG mode is defined by addresses 0 - 15 Table B1 and is repeated in addresses 16 - 111. The data from Display Memories 3 - 5 is directly transmitted to PROM outputs 01 - 03 to provide 8 video output states. The data from Display Memory 2 has no effect on the PROM output. A logic 0000 output is the darkest video state and a logic 1110 is the brightest state.

b. Sixteen (16) Shades-of-Grey (SOG) Video

The 16 SOG mode is defined by addresses 112 through 127 of Table B1. There is a direct correspondence between the address inputs A0 - A3 and outputs 00 - 03 to provide 16 video output states.

c. Eight (8) Shades-of-Grey (SOG) Sliding Grey Scale Video

The 8 SOG sliding grey scale is defined by addresses 128 to 255 of Table B1. Under the sliding grey scale operation, there are 8 modes each of which provides a distinct mapping correspondence between the 16 states defined by the four data address lines, A0 - A3, and an 8 SOG video output on lines 01 - 03. This mode of operation is used to provide increased contrast range over portions of a displayed map which would normally be displayed in the 16 SOG mode. In this mode of operation, the display mode would first be selected by the CPU over address lines A4 - A7. If mode 0 was selected (addresses 128 - 143), the lower 8 states of a 16 SOG display format which constitute approximately 1/2 the brightness dynamic range are mapped to 8 new SOGs which comprise the full dynamic range of video brightness output for expanded contrast range. The seven other sliding grey scale modes of operation each performs a similar function on an 8 successive state segment of a 16 SOG map.

APPENDIX C

CONTROL WORDS - FUNCTIONAL DESCRIPTION

This appendix gives a complete description, in paragraph a-c below, of the Control Words used to direct the operation of the DVC from the host SKC Computer. A total of four words are used to perform the control function, and their mode of entry and storage in the DVC is described in the main body of the report.

a. Control Words 0, 1 Display Mode

These two words set the operational status of the DVC when operating in the display mode.

Definition of Control Word Elements for Control Word 0, (Figure C1)

Byte Ø

Bits 0-3 Control Function Select must be ØØØØ to indicate first Control Word for Display function.

Bit 4 Synchronization Select

0 = External Synchronization
1 = Internal Synchronization

Bit 5 Resolution Select

0 = 256 pixels/line
1 = 512 pixels/line

Bit 6 Symbol Brightness

0 = Black symbols/alphanumerics
1 = White symbols/alphanumerics

Bit 7 Not used

Byte 1

Bit 0 Determines if Monitor 1 External Video Mixer Sources are to be left on when map is turned off.

0 = External Video Mixer Sources to be turned off
1 = External Video Mixer Sources to be left on

Bits 1 - 6 Monitor 1 Display Memory Select for B/w Mode

Display Memory Select (Bit No)	Display Status
6 5 4 3 2 1	
0 0 0 0 0 0	No Memories Displayed (blank screen)
0 0 0 0 0 1	Display Memory 1
0 0 0 0 1 0	Display Memory 2
0 0 0 1 0 0	Display Memory 3
0 0 1 0 0 0	Display Memory 4
0 1 0 0 0 0	Display Memory 5
1 0 0 0 0 0	Display Alphanumeric Page

The Display Memories may be selected in any combination, for example:

0 1 0 0 1 0	Displays the contents of Memories 2 & 5

Bit 7 Not used

Byte 2 - External Video Mixer Select

Video Mixer Select	Video Mixer Status
Bit No	
3 2 1 0	(bit number, for Monitor 1)
7 6 5 4	(bit number, for Monitor 2)
0 0 0 0	No External Video
0 0 0 1	External Source 1
0 0 1 0	External Source 2
0 1 0 0	External Source 3
1 0 0 0	External Source 4

External Sources can be selected in any combination, for example:

1 0 0 1 selects sources 1 and 4

Byte 3

Bit 0 Determines if Monitor 2 External Video Mixer Sources are to be left on when map is turned off

0 = External Video Sources to be turned off
1 = External Video Sources to be left on

Bits 1 - 6 Monitor 2 Display Memory Select for B/W Mode

Use the same truth table as Monitor 1 Display Memory Select for B/W Mode.

Definition of Control Word Elements for Control Word 1, (Figure C2)

Byte Ø

Bits 0 - 3 Control Function Select

Must be 0001 to indicate second Control Word for Display Function

Bits 4 - 7 Not Used

Byte 1

Bit 0 Not Used

Bits 1 - 4 Shades of Grey Select Code for map presentation

Bit No	Shades of Grey Mode
4 3 2 1	
0 X X X	3 Shades of Grey
1 0 0 0	4 Shades of Grey Mode 0
1 0 0 1	Shades of Grey Mode 1
1 0 1 0	Shades of Grey Mode 2
1 0 1 1	Shades of Grey Mode 3
1 1 0 0	Shades of Grey Mode 4
1 1 0 1	Shades of Grey Mode 5
1 1 1 0	Shades of Grey Mode 6
1 1 1 1	Shades of Grey Mode 7

See Map PROM Truth Table for more detail on each map mode

Bit 5 Display Map on Monitor 1

0 = NO
1 = YES

Bit 6 Display Map on Monitor 2

0 = NO
1 = YES

Bit 7 Determines the display status of the Alphanumeric Page for Monitor 1 when the map is turned off

0 = turn off Alphanumeric Page
1 = turn on Alphanumeric Page

<u>Byte 2</u>

Bit 0 Determines the display status of the Alphanumeric Page for Monitor 2 when the map is turned off

0 = turn off Alphanumeric Page
1 = turn on Alphanumeric Page

Bit 1 Update Alphanumeric Page

0 = NO
1 = YES

NOTE: Alphanumeric Page is updated prior to display of map.

Bit 2 Message select for updating Alphanumeric Page

0 = lower Display Memory Message
1 = upper Display Memory Message

Bit 3 - 7 Update Source Display Memory for Alphanumeric Page Update

Bit No	Display Memory Select
7 6 5 4 3	
0 0 0 0 1	Display Memory 1
0 0 0 1 0	Display Memory 2
0 0 1 0 0	Display Memory 3
0 1 0 0 0	Display Memory 4
1 0 0 0 0	Display Memory 5

Byte 3

Bit 0 Clear Alphanumeric Page

0 = NO
1 = YES

NOTE: Alphanumeric Page is cleared upon map display turn-off

Bit 1 Preset Display Memory

0 = NO
1 = YES

NOTE: Display Memories are preset upon map display turn-off

Bit 2 Display Memory Preset Data

0 will write 0s into selected Display Memories
1 will write 1s into selected Display Memories

Bits 3 - 7 Display Memory select for preset

Bit No	Display Memory Select
7 6 5 4 3	
0 0 0 0 1	1
0 0 0 1 0	2
0 0 1 0 0	3
0 1 0 0 0	4
1 0 0 0 0	5

Display Memories can be selected in any combination for preset, for example 1 0 0 0 1 selects Display Memories 1 and 5 for preset.

b. Control Word 2, Memory Preset/Clear

This control word presets/clears selected memories within the DVC.

Definition of Control Word Elements (Figure C3)

Byte Ø and Byte 1

Bits 0 - 3 Control Function Select
Must be ØØ1Ø to indicate memory preset/clear function

Bit 4 Clear Alphanumeric Page

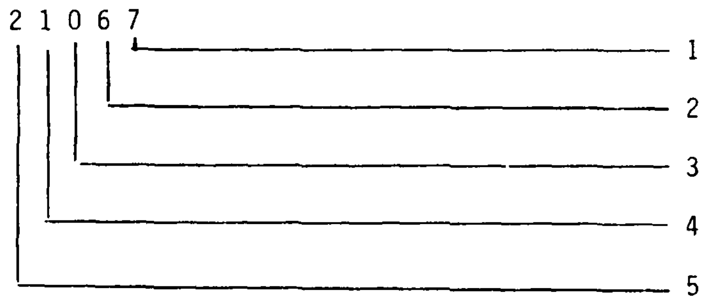
0 = NO
1 = YES

Bit 5 Resolution Select for presetting of Display Memories. In the 256 pixels/line mode only the section of the Display Memory relevant to 256 pixel/line storage is preset. In the 512 pixels/line mode the entire Display Memory is preset.

0 = 256 pixels/line
1 = 512 pixels/line

Byte Ø Bits 6, 7)
Byte 1 Bits 0 - 2) Preset Data for Display Memories

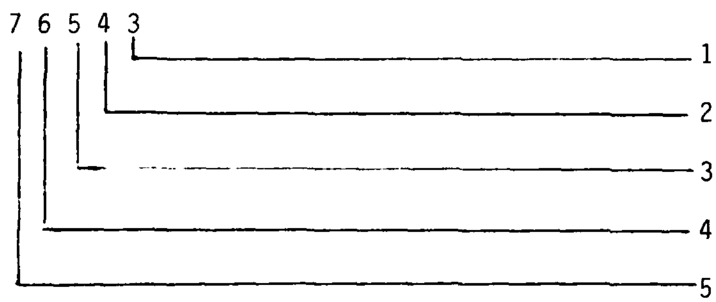
Byte 1 Byte Ø Display Memory No



0 will place logical 0s in the Display Memory
1 will place logical 1s in the Display Memory

Byte 1 Bits 3 - 7 Display Memory Select for preset

Bit No Display Memory Select

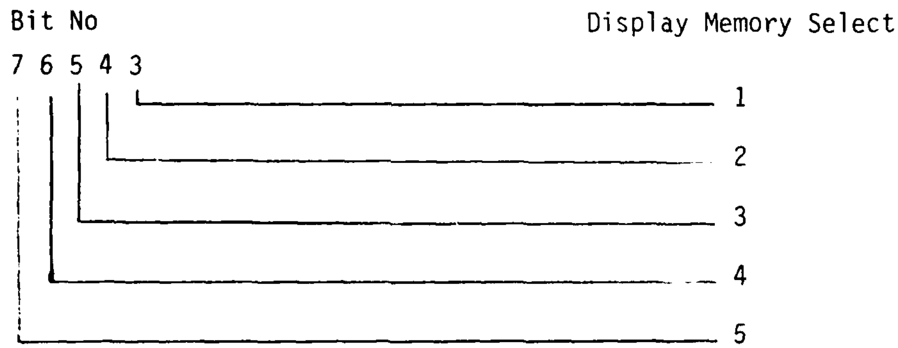


0 Display Memory will not be selected for preset
1 Display Memory will be selected for preset

Byte 2

Bits 0 - 2 Not Used

Bits 3 - 7 Clears Lower Alphanumeric Message of Selected Display Memories



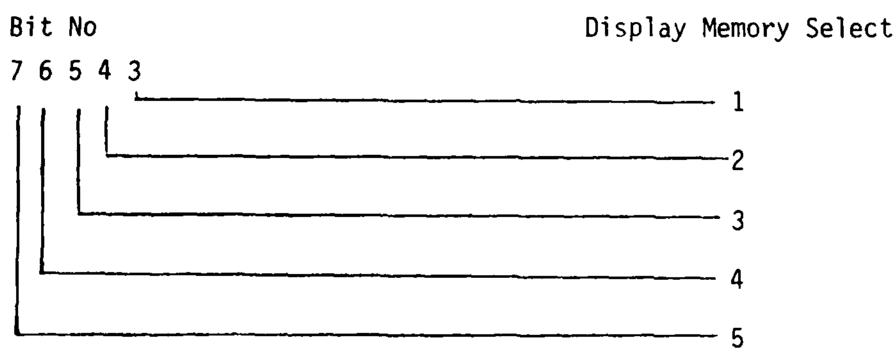
0 Lower Alphanumeric Message of Display Memory will not be selected for clearing.

1 Lower Alphanumeric Message of Display Memory will be selected for clearing.

Byte 3

Bits 0 - 2 Not Used

Bits 3 - 7 Clears Upper Alphanumeric Message of selected Display Memories



0 Lower Alphanumeric Message of Display Memory will not be selected for clearing.

1 Lower Alphanumeric Message of Display Memory will be selected for clearing.

c. Control Word 3, Modify Alphanumeric Data

This word modifies or clears contents of Alphanumeric Page Memory.

Definition of Control Word Elements (Figure C4)

<u>Byte Ø</u>

Bits 0 - 3 Control Function Select
Must be ØØ11 to indicate Modify Alphanumeric Data Function

Bits 4, 5 Not Used

Bits 6 Displays contents of Alphanumeric Page Memory on Monitor 1 after Alphanumeric Page update.

0 = NO
1 = YES

Bit 7 Displays contents of Alphanumeric Page Memory on Monitor 2 after Alphanumeric Page update.

0 = NO
1 = YES

<u>Byte 1</u>

Bit 0 Update Alphanumeric Page Memory

0 = NO
1 = YES

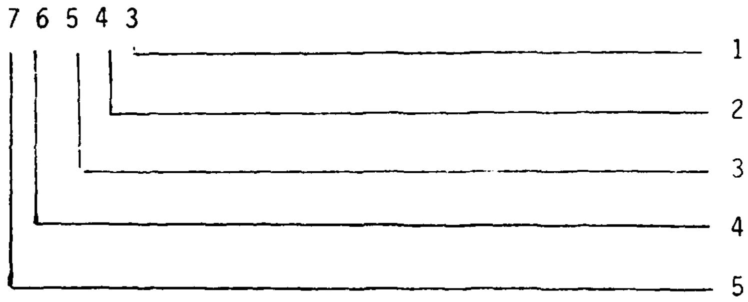
Bit 1 Not Used

Bit 2 Message select from selected Display Memory

0 = Lower Message
1 = Upper Message

Bits 3 - 7 Display Memory source for updating of Alphanumeric Page Memory

Bit No Display Memory Selected



<u>Byte 2</u>

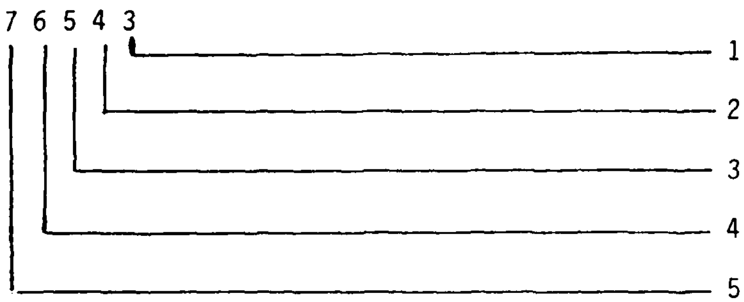
Bit 0 Clear Alphanumeric Page

0 = NO
1 = YES

Bits 1, 2 Not Used

Bits 3 - 7 Display Memory select for clearing of Alphanumeric messages. Both Lower and Upper Messages are cleared in each selected Display Memory.

Bit No Display Memory Select



<u>Byte 3</u> Not Used

TABLE 1

DIGITAL TO VIDEO CONVERTER MEMORY ORGANIZATION

ADDRESS: Binary Bit No.	ADDRESS: Hexadecimal	Memory Type	Data Field Width
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	3 2 1 0		
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	CPU EPROM	8 Bit
⋮	⋮		
0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1	5 7 F F		
0 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0	5 8 0 0	CPU RAM	8 Bit
⋮	⋮		
0 1 0 1 1 0 1 1 1 1 1 1 1 1 1 1	5 B F F		
0 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0	5 C 0 0	ALPHANUMERIC PAGE RAM	8 Bit
⋮	⋮		
0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	5 F F F		
0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	6 0 0 0	DISPLAY MEMORY 1 (RAM)	32 Bit
⋮	⋮		
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	7 F F F		
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	8 0 0 0	DISPLAY MEMORY 2 (RAM)	32 Bit
⋮	⋮		
1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	9 F F F		
1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	A 0 0 0	DISPLAY MEMORY 3 (RAM)	32 Bit
⋮	⋮		
1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	B F F F		
1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	C 0 0 0	DISPLAY MEMORY 4 (RAM)	32 Bit
⋮	⋮		
1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	D F F F		
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	E 0 0 0	DISPLAY MEMORY 5 (RAM)	32 Bit
⋮	⋮		
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	F F F F		

NOTES:

1. CPU EPROM Memory - 22K of EPROM is available for use by the DVC. This memory stores the DVC system operating program. It is accessible only from the CPU and not from the SKC Computer. This memory utilizes 2716 EPROM integrated circuits.

2. CPU RAM Memory - 1K of RAM is available for use by the DVC CPU. The memory is only available to the DVC CPU for temporary storage of operational data and computations. The memory utilizes 2114 static RAM integrated circuits.

3. Alphanumeric Page RAM Memory - 1K of RAM is utilized in the Alphanumeric Page Memory. It is only accessible from the DVC CPU and is used to store the alphanumeric data presently being displayed. This memory utilizes 2114 static RAM integrated circuits.

4. Display Memories 1-5 - Each display memory consists of 8K of dynamic RAM memory. These memories are used to store both symbolic and shades-of-grey display data. They are accessible from both the CPU and the SKC computer. These memories utilize 2108 dynamic RAM integrated circuits.

TABLE 2

DISPLAY MEMORY ALLOCATION, FIELD Ø, 512 PIXELS/LINE RESOLUTION

Display Line No.	Word No.	Binary Bit No. (ADDRESS 1, 2) 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal 3 2 1 0
0	0	S S S 0	0 0 0 0	0 0 0 0	0 0 0 0	M 0 0 0
	1	S S S 0	0 0 0 0	0 0 0 0	0 0 0 1	M 0 0 1
	⋮			⋮		⋮
	15	S S S 0	0 0 0 0	0 0 0 0	1 1 1 1	M 0 0 F
2	0	S S S 0	0 0 0 0	0 0 1 0	0 0 0 0	M 0 2 0
	⋮			⋮		⋮
	15	S S S 0	0 0 0 0	0 0 1 0	1 1 1 1	M 0 2 F
4	0	S S S 0	0 0 0 0	0 1 0 0	0 0 0 0	M 0 4 0
	⋮			⋮		⋮
	15	S S S 0	0 0 0 0	0 1 0 0	1 1 1 1	M 0 4 F
	⋮			⋮		⋮
478	0	S S S 1	1 1 0 1	1 1 1 0	0 0 0 0	N 0 E 0
	⋮			⋮		⋮
	15	S S S 1	1 1 0 1	1 1 1 0	1 1 1 1	N 0 E F

1. Binary address bits 13-15 (labeled SSS) form the Display Memory Select Code. The Memory Select Codes are:

Address Bit No. 15	14	13	Display Memory Selected
0	1	1	1
1	0	0	2
1	0	1	3
1	1	0	4
1	1	1	5

2. The Display Memory selection is reflected in the third digit of the address when specified in a hexadecimal format. In addition, the twelfth address bit which is part of this digit is used in the data address field. Thus to compute the value of M or N in the tables, both the desired memory select code and data address must be utilized.

TABLE 3

DISPLAY MEMORY ALLOCATION, FIELD 1, 512 PIXELS/LINE RESOLUTION

Display Line No.	Word No.	Binary Bit No. 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal ADDRESS [1] 3 2 1 0
1	0	S S S 0	0 0 0 0	0 0 0 1	0 0 0 0	M 0 1 0
	1	S S S 0	0 0 0 0	0 0 0 1	0 0 0 1	M 0 1 1
	⋮		⋮			⋮
	15	S S S 0	0 0 0 0	0 0 0 1	1 1 1 1	M 0 1 F
3	0	S S S 0	0 0 0 0	0 0 1 1	0 0 0 0	M 0 3 0
	⋮		⋮			⋮
	15	S S S 0	0 0 0 0	0 0 1 1	1 1 1 1	M 0 3 F
5	0	S S S 0	0 0 0 0	0 1 0 1	0 0 0 0	M 0 5 0
	⋮		⋮			⋮
	15	S S S 0	0 0 0 0	0 1 0 1	1 1 1 1	M 0 5 F
	⋮		⋮			⋮
479	0	S S S 1	1 1 0 1	1 1 1 1	0 0 0 0	M D F 0
	⋮		⋮			⋮
	15	S S S 1	1 1 0 1	1 1 1 1	1 1 1 1	M D F F

1. Refer to the footnotes of Table 2.

TABLE 4

DISPLAY MEMORY ALLOCATION 256 PIXELS/LINE RESOLUTION

ADDRESS 1

Display Line No.	Word No.	Binary Bit No. 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal 3 2 1 0
0	0	S S S 0	0 0 0 0	0 0 0 0	0 0 0 0	M 0 0 0
	1	S S S 0	0 0 0 0	0 0 0 0	0 0 1 0	M 0 0 2
	2	S S S 0	0 0 0 0	0 0 0 0	0 1 0 0	M 0 0 4
	3	S S S 0	0 0 0 0	0 0 0 0	0 1 1 0	M 0 0 6
	⋮			⋮		⋮
	7	S S S 0	0 0 0 0	0 0 0 0	1 1 1 0	M 0 0 E
1	0	S S S 0	0 0 0 0	0 0 0 1	0 0 0 0	M 0 1 0
	⋮			⋮		⋮
	7	S S S 0	0 0 0 0	0 0 0 1	1 1 1 0	M 0 1 E
2	0	S S S 0	0 0 0 0	0 0 1 0	0 0 0 0	M 0 2 0
	⋮			⋮		⋮
	7	S S S 0	0 0 0 0	0 0 1 0	1 1 1 0	M 0 2 E
3	0	S S S 0	0 0 0 0	0 0 1 1	0 0 0 0	M 0 3 0
	⋮			⋮		⋮
	7	S S S 0	0 0 0 0	0 0 1 1	1 1 1 0	M 0 3 E
	⋮			⋮		⋮
239		S S S 0	1 1 1 0	1 1 1 1	0 0 0 0	M E F 0
	⋮			⋮		⋮
	7	S S S 0	1 1 1 0	1 1 1 1	1 1 1 0	M E F E

1. Refer to the footnotes of Table 2.

TABLE 5

ALPHANUMERIC MESSAGE STORAGE ALLOCATION IN DISPLAY MEMORIES

LOWER MESSAGE

ADDRESS 1, 2

Line No.	Characters (4 EA)	Binary Bit No. 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal 3 2 1 0
(Map Data Storage) (512 Pixels/Line) (Odd + Even Field)		S S S 0	0 0 0 0	0 0 0 0	0 0 0 0	M 0 0 0
				⋮		⋮
		S S S 1	1 1 0 1	1 1 1 1	1 1 1 1	N D F F
0	3-0	S S S 1	1 1 1 0	0 0 0 0	0 0 0 0	N E 0 0
	7-4	S S S 1	1 1 1 0	0 0 0 0	0 0 0 1	N E 0 1
	⋮			⋮		⋮
	63-60	S S S 1	1 1 1 0	0 0 0 0	1 1 1 1	N E 0 F
1	3-0	S S S 1	1 1 1 0	0 0 0 1	0 0 0 0	N E 1 0
	⋮			⋮		⋮
	63-60	S S S 1	1 1 1 0	0 0 0 1	1 1 1 1	N E 1 F
⋮						
14	3-0	S S S 1	1 1 1 0	1 1 1 0	0 0 0 0	N E E 0
	⋮			⋮		⋮
	63-60	S S S 1	1 1 1 0	1 1 1 0	1 1 1 1	N E E F

1. The Upper Alphanumeric Message is addressed by changing hexadecimal Address No. 2 from an E to an F.

2. Refer to the footnotes of Table 2.

TABLE 6

CPU/ALPHANUMERIC PAGE MEMORY ORGANIZATION

ADDRESS Binary Bit No. 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal 3 2 1 0	Memory Type	Availability
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	EPROM 2716	On Board, In Sockets
⋮				⋮		
0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1	1 F F F		
0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	2 0 0 0	Not wired, can be used for EPROM or RAM	
⋮				⋮		
0 1 0 1	0 1 1 1	1 1 1 1	1 1 1 1	5 7 F F		
0 1 0 1	1 0 0 0	0 0 0 0	0 0 0 0	5 8 0 0	Static RAM 2114	On Board, Hard wired
⋮				⋮		
0 1 0 1	1 0 1 1	1 1 1 1	1 1 1 1	5 B F F		
0 1 0 1	1 1 0 0	0 0 0 0	0 0 0 0	5 C 0 0	Alphanumeric Page, Static RAM 2114	On Board, In Sockets
⋮				⋮		
0 1 0 1	1 1 1 1	1 0 1 1	1 1 1 1	5 F B F		
0 1 0 1	1 1 1 1	1 1 0 0	0 0 0 0	5 F C 0	Not used - Upper Part of Alphanumeric Page	On Board, In Sockets
⋮				⋮		
0 1 0 1	1 1 1 1	1 1 1 1	1 1 1 1	5 F F F		

TABLE 7

EXPANDED ALPHANUMERIC PAGE MEMORY ALLOCATION

Line No.	Character No.	ADDRESS Binary Bit No. 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hexadecimal 3 2 1 0
0	0	0 1 0 1	1 1 0 0	0 0 0 0	0 0 0 0	5 C 0 0
	1	0 1 0 1	1 1 0 0	0 0 0 0	0 0 0 1	5 C 0 1
	⋮	⋮				⋮
	63	0 1 0 1	1 1 0 0	0 0 1 1	1 1 1 1	5 C 3 F
1	0	0 1 0 1	1 1 0 0	0 1 0 0	0 0 0 0	5 C 4 0
	1	0 1 0 1	1 1 0 0	0 1 0 0	0 0 0 1	5 C 4 1
	⋮	⋮				⋮
	63	0 1 0 1	1 1 0 0	0 1 1 1	1 1 1 1	5 C 7 F
⋮		⋮				⋮
14	0	0 1 0 1	1 1 1 1	1 0 0 0	0 0 0 0	5 F 8 0
	⋮	⋮				⋮
	63	0 1 0 1	1 1 1 1	1 0 1 1	1 1 1 1	5 F B F

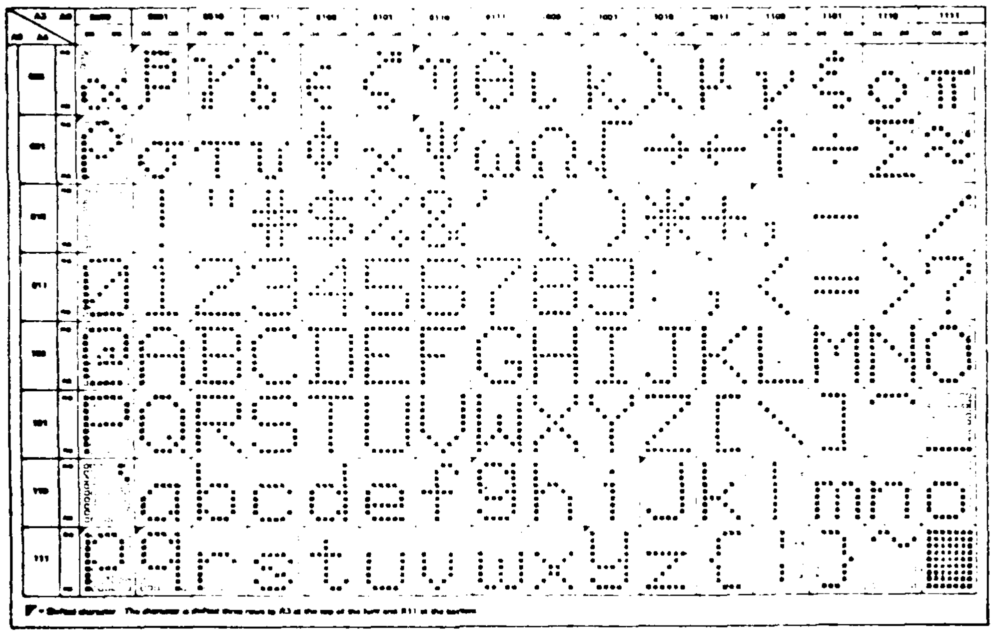


TABLE 8. MCM 6571AL Display Pattern Table Shifted ASCII Characters and Greek.

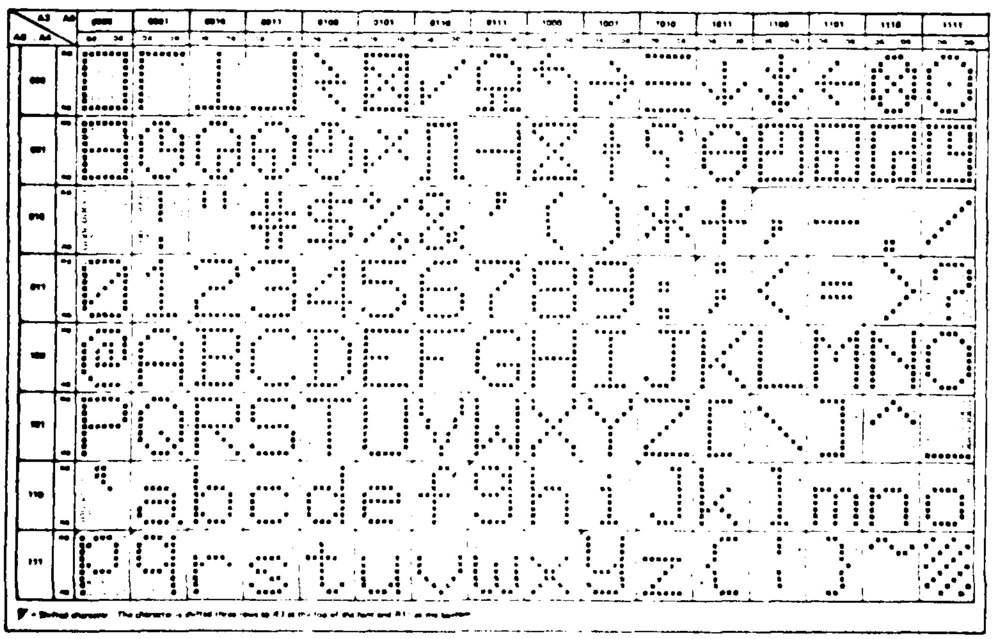


TABLE 9. MCM6574L Display Pattern Table Math Symbols and Pictures.

TABLE A1

MAP DISPLAY MODE STATE TABLE

Trigger Commands	Map Display Mode
1	8 SOG Sliding Grey Scale Mode 0
2	8 SOG Sliding Grey Scale Mode 1
3	8 SOG Sliding Grey Scale Mode 2
4	8 SOG Sliding Grey Scale Mode 3
5	8 SOG Sliding Grey Scale Mode 4
6	8 SOG Sliding Grey Scale Mode 5
7	8 SOG Sliding Grey Scale Mode 6
8	8 SOG Sliding Grey Scale Mode 7
9	8 SOG Non-Sliding Grey Scale
10	16 SOG
11	16 SOG
12	16 SOG
13	16 SOG
14	16 SOG
15	16 SOG
16	16 SOG
17	Repeat table starting with Trigger Command 1.

TABLE B1

MAP VIDEO PROM TRUTH TABLE

MAP VIDEO PROM [illegible]

ADVANCED MICRO DEVICES [illegible]

DATA [illegible]

O0	-	VIDEO OUTPUT	0	TO VIDEO OUTPUT LATCH	A
O1	-	VIDEO OUTPUT	1	TO VIDEO OUTPUT LATCH	B
O2	-	VIDEO OUTPUT	2	TO VIDEO OUTPUT LATCH	C
O3	-	VIDEO OUTPUT	3	TO VIDEO OUTPUT LATCH	D

ADDRESSES

A0	-	DATA INPUT	0	FROM MEMORY	2
A1	-	DATA INPUT	1	FROM MEMORY	3
A2	-	DATA INPUT	2	FROM MEMORY	4
A3	-	DATA INPUT	3	FROM MEMORY	5
A4	-	MAP CONTROL 1		FROM MAP DISPLAY REGISTER	01
A5	-	MAP CONTROL 2		FROM MAP DISPLAY REGISTER	02
A6	-	MAP CONTROL 3		FROM MAP DISPLAY REGISTER	03
A7	-	MAP CONTROL 4		FROM MAP DISPLAY REGISTER	04
CS1/	-	GND			

NOTE: HEX ADDRESSES USE THE LETTER "Z" FOLLOWING "A"

ADDR	HEX ADDR	A LINES (7-0)	D(3-0)	CONTROL	COMMENTS
0	00	0000 0000	0000	[illegible]	3 DATA LINE 8 SHADES GREY MAP
1	01	0000 0001	0000	[illegible]	
2	02	0000 0010	0010	[illegible]	
3	03	0000 0011	0010	[illegible]	
4	04	0000 0100	0100	[illegible]	
5	05	0000 0101	0100	[illegible]	
6	06	0000 0110	0110	[illegible]	
7	07	0000 0111	0110	[illegible]	
8	08	0000 1000	1000	[illegible]	
9	09	0000 1001	1000	[illegible]	
10	0A	0000 1010	1010	[illegible]	
11	0Z	0000 1011	1010	[illegible]	
12	0C	0000 1100	1100	[illegible]	
13	0D	0000 1101	1100	[illegible]	
14	0E	0000 1110	1110	[illegible]	
15	0F	0000 1111	1110	[illegible]	
16	10	0001 0000	0000	[illegible]	3 DATA LINE 8 SHADES GREY MAP
17	11	0001 0001	0000	[illegible]	
18	12	0001 0010	0010	[illegible]	
19	13	0001 0011	0010	[illegible]	
20	14	0001 0100	0100	[illegible]	
21	15	0001 0101	0100	[illegible]	
22	16	0001 0110	0110	[illegible]	
23	17	0001 0111	0110	[illegible]	
24	18	0001 1000	1000	[illegible]	
25	19	0001 1001	1000	[illegible]	
26	1A	0001 1010	1010	[illegible]	
27	1Z	0001 1011	1010	[illegible]	
28	1C	0001 1100	1100	[illegible]	
29	1D	0001 1101	1100	[illegible]	
30	1E	0001 1110	1110	[illegible]	
31	1F	0001 1111	1110	[illegible]	

TABLE B1 - CONTINUED

ADDR	HEX ADDR	A LINES [illegible]	[illegible]	[illegible]	
32	20	0010 0000	0000	BHHHHH	3 DATA LINE 8 SHADES GREY MAP
33	21	0010 0001	0000	BHHHHH	
34	22	0010 0010	0010	BHHHFH	
35	23	0010 0011	0010	BHHHFH	
36	24	0010 0100	0100	BHHFHH	
37	25	0010 0101	0100	BHHFHH	
38	26	0010 0110	0110	BHHFFH	
39	27	0010 0111	0110	BHHFFH	
40	28	0010 1000	1000	BHFHHH	
41	29	0010 1001	1000	BHFHHH	
42	2A	0010 1010	1010	BHFHFH	
43	2B	0010 1011	1010	BHFHFH	
44	2C	0010 1100	1100	BHFFHH	
45	2D	0010 1101	1100	BHFFHH	
46	2E	0010 1110	1110	BHFFFH	
47	2F	0010 1111	1110	BHFFFH	
48	30	0011 0000	0000	BHHHHH	3 DATA LINE 8 SHADES-GREY MAP
49	31	0011 0001	0000	BHHHHH	
50	32	0011 0010	0010	BHHHFH	
51	33	0011 0011	0010	BHHHFH	
52	34	0011 0100	0100	BHHFHH	
53	35	0011 0101	0100	BHHFHH	
54	36	0011 0110	0110	BHHFFH	
55	37	0011 0111	0110	BHHFFH	
56	38	0011 1000	1000	BHFHHH	
57	39	0011 1001	1000	BHFHHH	
58	3A	0011 1010	1010	BHFHFH	
59	3B	0011 1011	1010	BHFHFH	
60	3C	0011 1100	1100	BHFFHH	
61	3D	0011 1101	1100	BHFFHH	
62	3E	0011 1110	1110	BHFFFH	
63	3F	0011 1111	1110	BHFFFH	
64	40	0100 0000	0000	BHHHHH	3 DATA LINE 8 SHADES GREY MAP
65	41	0100 0001	0000	BHHHHH	
66	42	0100 0010	0010	BHHHFH	
67	43	0100 0011	0010	BHHHFH	
68	44	0100 0100	0100	BHHFHH	
69	45	0100 0101	0100	BHHFHH	
70	46	0100 0110	0110	BHHFFH	
71	47	0100 0111	0110	BHHFFH	
72	48	0100 1000	1000	BHFHHH	
73	49	0100 1001	1000	BHFHHH	
74	4A	0100 1010	1010	BHFHFH	
75	4B	0100 1011	1010	BHFHFH	
76	4C	0100 1100	1100	BHFFHH	
77	4D	0100 1101	1100	BHFFHH	
78	4E	0100 1110	1110	BHFFFH	
79	4F	0100 1111	1110	BHFFFH	

TABLE B1 - CONTINUED

ADDR	HEX ADDR	A LINES (7-0)	D(3-0)	CONTROL	COMMENTS
80	50	0101 0000	0000	BNNNNN	1 DATA LINE 8 SHADES GREY MAP
81	51	0101 0001	0000	BNNNNN	
82	52	0101 0010	0010	BNNNFN	
83	53	0101 0011	0010	BNNNFN	
84	54	0101 0100	0100	BNFNNF	
85	55	0101 0101	0100	BNFNNN	
86	56	0101 0110	0110	BNFFNF	
87	57	0101 0111	0110	BNFFNF	
88	58	0101 1000	1000	BFNNNF	
89	59	0101 1001	1000	BFNNNF	
90	5A	0101 1010	1010	BFNFNF	
91	5B	0101 1011	1010	BFNFNF	
92	5C	0101 1100	1100	BFFNNF	
93	5D	0101 1101	1100	BFFNNN	
94	5E	0101 1110	1110	BFFFNN	
95	5F	0101 1111	1110	BFFFNN	
96	60	0110 0000	0000	BNNNNN	3 DATA LINE 8 SHADES GREY MAP
97	61	0110 0001	0000	BNNNNF	
98	62	0110 0010	0010	BNNFNF	
99	63	0110 0011	0010	BNNFNF	
100	64	0110 0100	0100	BNFNNF	
101	65	0110 0101	0100	BNFNNN	
102	66	0110 0110	0110	BNFFNF	
103	67	0110 0111	0110	BNFFNF	
104	68	0110 1000	1000	BFNNNF	
105	69	0110 1001	1000	BFNNNF	
106	6A	0110 1010	1010	BFNFNF	
107	6B	0110 1011	1010	BFNFNF	
108	6C	1100 1100	0110	BFFNNF	
109	6D	1100 1101	0110	BFFNNN	
110	6E	0110 1110	1110	BFFFNF	
111	6F	0110 1111	1110	BFFFNF	
112	70	0111 0000	0000	BNNNNF	4 DATA LINE 16 SHADES GREY MAP
113	71	0111 0001	0001	BNNNFF	
114	72	0111 0010	0010	BNNFNF	
115	73	0111 0011	0011	BNNFFF	
116	74	0111 0100	0100	BNFNNF	
117	75	0111 0101	0101	BNFNFF	
118	76	0111 0110	0110	BNFFNF	
119	77	0111 0111	0111	BNFFFF	
120	78	0111 1000	1000	BFNNNF	
121	79	0111 1001	1001	BFNNFF	
122	7A	0111 1010	1010	BFNFNF	
123	7B	0111 1011	1011	BFNFFF	
124	7C	0111 1100	1100	BFFNNF	
125	7D	0111 1101	1101	BFFNFF	
126	7E	0111 1110	1110	BFFFNF	
127	7F	0111 1111	1111	BFFFFF	

TABLE B1 - CONTINUED

ADDR	HEX ADDR	A LINES [illegible]	[illegible]	CONTROL	COMMENTS
128	80	1000 0000	[illegible]	[illegible]	1 DATA LINE 8 SHADES GREY MAP
129	81	1000 0001	[illegible]	[illegible]	
130	82	1000 0010	0010	[illegible]	MODE 0 SLIDING SCALE
131	83	1000 0011	0100	[illegible]	
132	84	1000 0100	0110	[illegible]	
133	85	1000 0101	1000	[illegible]	
134	86	1000 0110	1010	[illegible]	
135	87	1000 0111	1100	[illegible]	
136	88	1000 1000	1110	[illegible]	
137	89	1000 1001	1110	[illegible]	
138	8A	1000 1010	1110	[illegible]	
139	8B	1000 1011	1110	[illegible]	
140	8C	1000 1100	1110	[illegible]	
141	8D	1000 1101	1110	[illegible]	
142	8E	1000 1110	1110	[illegible]	
143	8F	1000 1111	1110	[illegible]	
144	90	1001 0000	0000	[illegible]	4 DATA LINE 8 SHADES GREY MAP
145	91	1001 0001	0000	[illegible]	
146	92	1001 0010	0000	[illegible]	MODE 1 SLIDING SCALE
147	93	1001 0011	0010	[illegible]	
148	94	1001 0100	0100	[illegible]	
149	95	1001 0101	0110	[illegible]	
150	96	1001 0110	1000	[illegible]	
151	97	1001 0111	1010	[illegible]	
152	98	1001 1000	1100	[illegible]	
153	99	1001 1001	1110	[illegible]	
154	9A	1001 1010	1110	[illegible]	
155	9B	1001 1011	1110	[illegible]	
156	9C	1001 1100	1110	[illegible]	
157	9D	1001 1101	1110	[illegible]	
158	9E	1001 1110	1110	[illegible]	
159	9F	1001 1111	1110	[illegible]	
160	A0	1010 0000	0000	[illegible]	4 DATA LINE 8 SHADES GREY MAP
161	A1	1010 0001	0000	[illegible]	
162	A2	1010 0010	0000	[illegible]	MODE 2 SLIDING SCALE
163	A3	1010 0011	0000	[illegible]	
164	A4	1010 0100	0010	[illegible]	
165	A5	1010 0101	0100	[illegible]	
166	A6	1010 0110	0110	[illegible]	
167	A7	1010 0111	1000	[illegible]	
168	A8	1010 1000	1010	[illegible]	
169	A9	1010 1001	1100	[illegible]	
170	AA	1010 1010	1110	[illegible]	
171	AB	1010 1011	1110	[illegible]	
172	AC	1010 1100	1110	[illegible]	
173	AD	1010 1101	1110	[illegible]	
174	AE	1010 1110	1110	[illegible]	
175	AF	1010 1111	1110	[illegible]	

TABLE B1 - CONTINUED

ADDR	HEX ADDR	A LINES(7-0)	D(3-0)	CONTROL	COMMENTS
176	B0	1011 0000	0000	BHHHHH	4 DATA LINE 8 SHADES GREY MAP
177	B1	1011 0001	0000	BHHHHH	
178	B2	1011 0010	0000	BHHHHH	MODE 3 SLIDING SCALE
179	B3	1011 0011	0000	BHHHHH	
180	B4	1011 0100	0000	BHHHHH	
181	B5	1011 0101	0010	BHHHFH	
182	B6	1011 0110	0100	BHHFHH	
183	B7	1011 0111	0110	BHFFHH	
184	B8	1011 1000	1000	BFHHHH	
185	B9	1011 1001	1010	BFHFHH	
186	BA	1011 1010	1100	BFFHHH	
187	BB	1011 1011	1110	BFFFHH	
188	BC	1011 1100	1110	BFFFHH	
189	BD	1011 1101	1110	BFFFHH	
190	BE	1011 1110	1110	BFFFHH	
191	BF	1011 1111	1110	BFFFHH	

ADDR	HEX ADDR	A LINES(7-0)	D(3-0)	CONTROL	COMMENTS
192	C0	1100 0000	0000	BHHHHF	4 DATA LINE 8 SHADES GREY MAP
193	C1	1100 0001	0000	BHHHHF	
194	C2	1100 0010	0000	BHHHHF	MODE 4 SLIDING SCALE
195	C3	1100 0011	0000	BHHHHF	
196	C4	1100 0100	0000	BHHHHF	
197	C5	1100 0101	0000	BHHHHF	
198	C6	1100 0110	0010	BHHHFHF	
199	C7	1100 0111	0100	BHFHHF	
200	C8	1100 1000	0110	BHFFHF	
201	C9	1100 1001	1000	BFHHHF	
202	CA	1100 1010	1010	BFHFHF	
203	CB	1100 1011	1100	BFFHHF	
204	CC	1100 1100	1110	BFFFHF	
205	CD	1100 1101	1110	BFFFHF	
206	CE	1100 1110	1110	BFFFHF	
207	CF	1100 1111	1110	BFFFHF	

ADDR	HEX ADDR	A LINES(7-0)	D(3-0)	CONTROL	COMMENTS
208	D0	1101 0000	0000	BHHHHH	4 DATA LINE 8 SHADES GREY MAP
209	D1	1101 0001	0000	BHHHHH	
210	D2	1101 0010	0000	BHHHHH	MODE 5 SLIDING SCALE
211	D3	1101 0011	0000	BHHHHH	
212	D4	1101 0100	0000	BHHHHH	
213	D5	1101 0101	0000	BHHHHH	
214	D6	1101 0110	0000	BHHHHH	
215	D7	1101 0111	0010	BHHHFH	
216	D8	1101 1000	0100	BHFHHH	
217	D9	1101 1001	0110	BHFFHH	
218	DA	1101 1010	1000	BFHHHH	
219	DB	1101 1011	1010	BFHFHH	
220	DC	1101 1100	1100	BFFHHH	
221	DD	1101 1101	1110	BFFFHH	
222	DE	1101 1110	1110	BFFFHH	
223	DF	1101 1111	1110	BFFFHH	

TABLE B1 - CONTINUED

ADDR	HEX ADDR	A LINES(7 0)	D(3 0)	CONTROL	COMMENTS
224	E0	1110 0000	0000	[illegible]	4 DATA LINE 8 SHADES GREY MAP
225	E1	1110 0001	0000	[illegible]	
226	E2	1110 0010	0000	[illegible]	MODE 6 SLIDING SCALE
227	E3	1110 0011	0000	[illegible]	
228	E4	1110 0100	0000	[illegible]	
229	E5	1110 0101	0000	[illegible]	
230	E6	1110 0110	0000	[illegible]	
231	E7	1110 0111	0000	[illegible]	
232	E8	1110 1000	0010	[illegible]	
233	E9	1110 1001	0100	[illegible]	
234	EA	1110 1010	0110	[illegible]	
235	EB	1110 1011	1000	[illegible]	
236	EC	1110 1100	1010	[illegible]	
237	ED	1110 1101	1100	[illegible]	
238	EE	1110 1110	1110	[illegible]	
239	EF	1110 1111	1110	[illegible]	
240	F0	1111 0000	0000	[illegible]	4 DATA LINE 8 SHADES GREY MAP
241	F1	1111 0001	0000	[illegible]	
242	F2	1111 0010	0000	[illegible]	MODE 7 SLIDING SCALE
243	F3	1111 0011	0000	[illegible]	
244	F4	1111 0100	0000	[illegible]	
245	F5	1111 0101	0000	[illegible]	
246	F6	1111 0110	0000	[illegible]	
247	F7	1111 0111	0000	[illegible]	
248	F8	1111 1000	0000	[illegible]	
249	F9	1111 1001	0010	[illegible]	
250	FA	1111 1010	0100	[illegible]	
251	FB	1111 1011	0110	[illegible]	
252	FC	1111 1100	1000	[illegible]	
253	FD	1111 1101	1010	[illegible]	
254	FE	1111 1110	1100	[illegible]	
255	FF	1111 1111	1110	[illegible]	

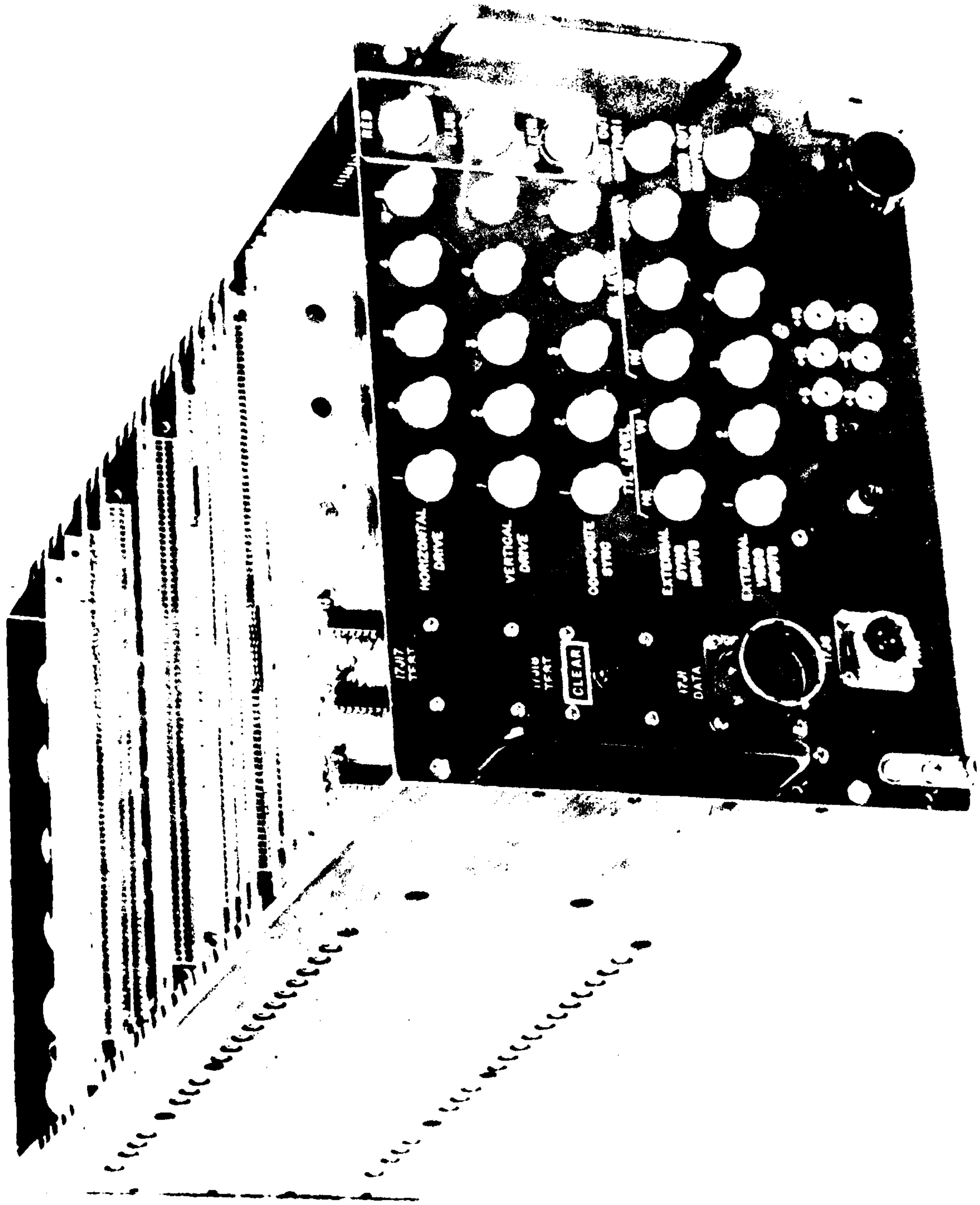


Figure 1. Digital to Video Converter

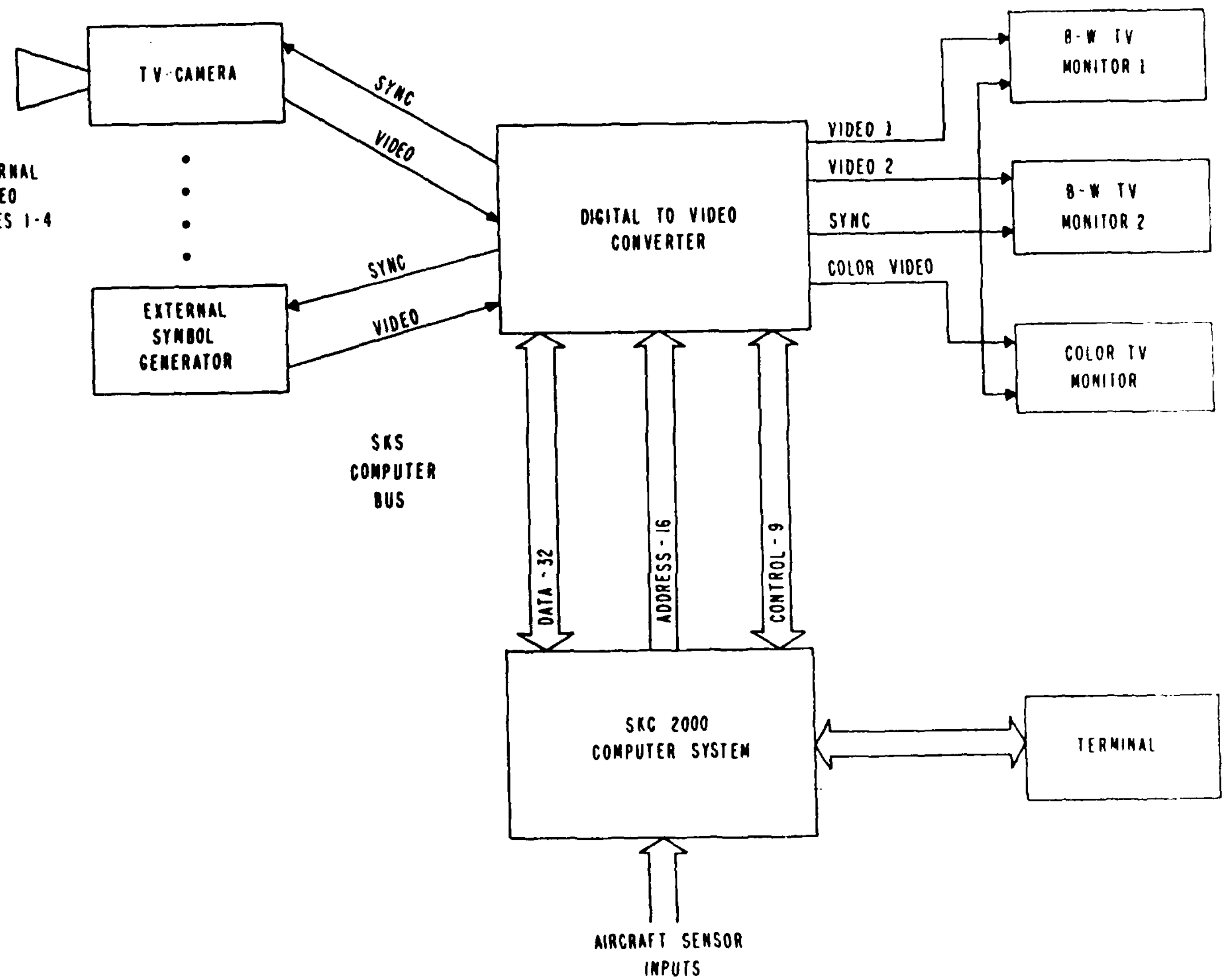


Figure 2. Block Diagram of Display System

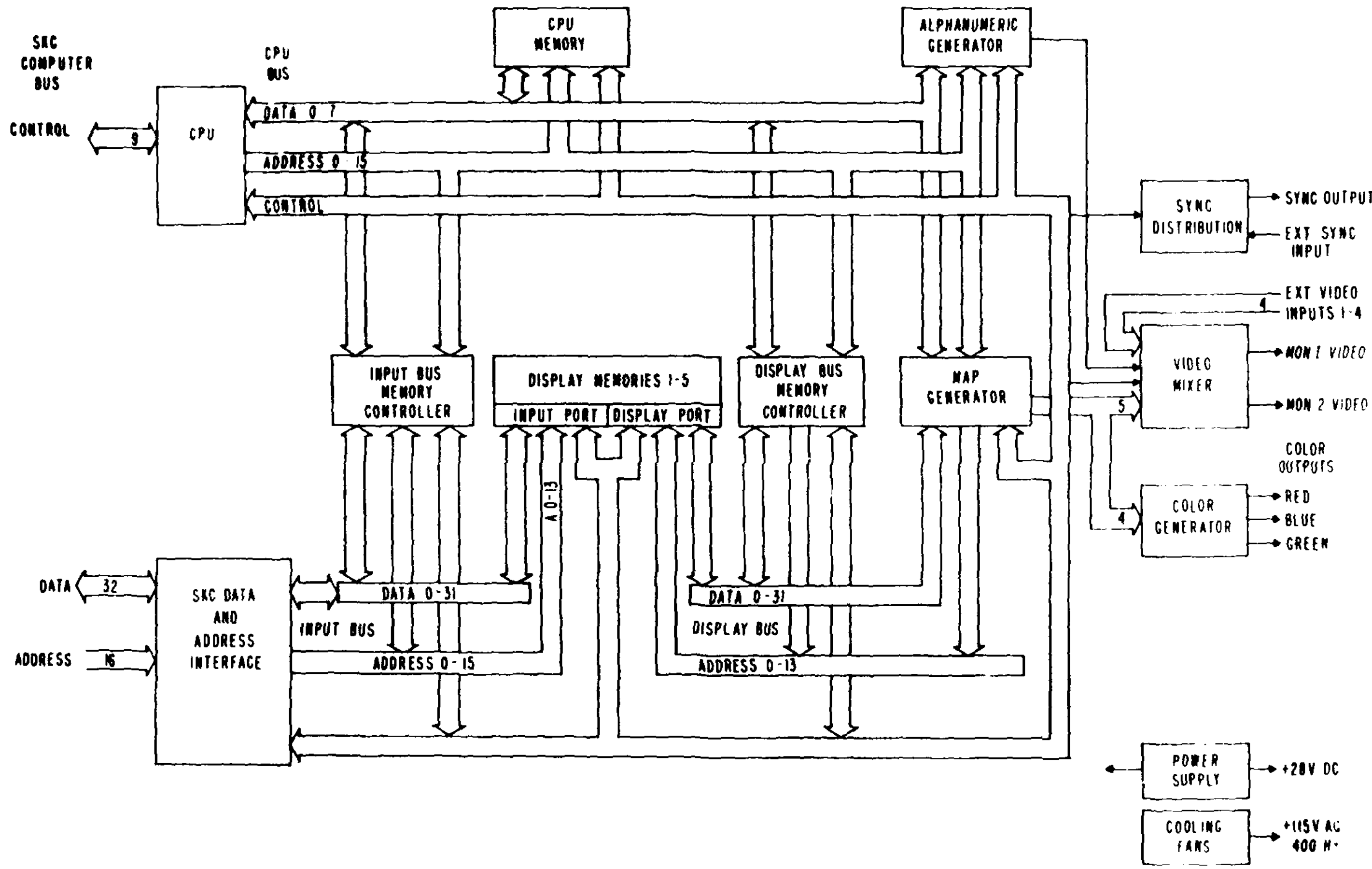


Figure 3. Simplified Block Diagram of Digital to Video Converter

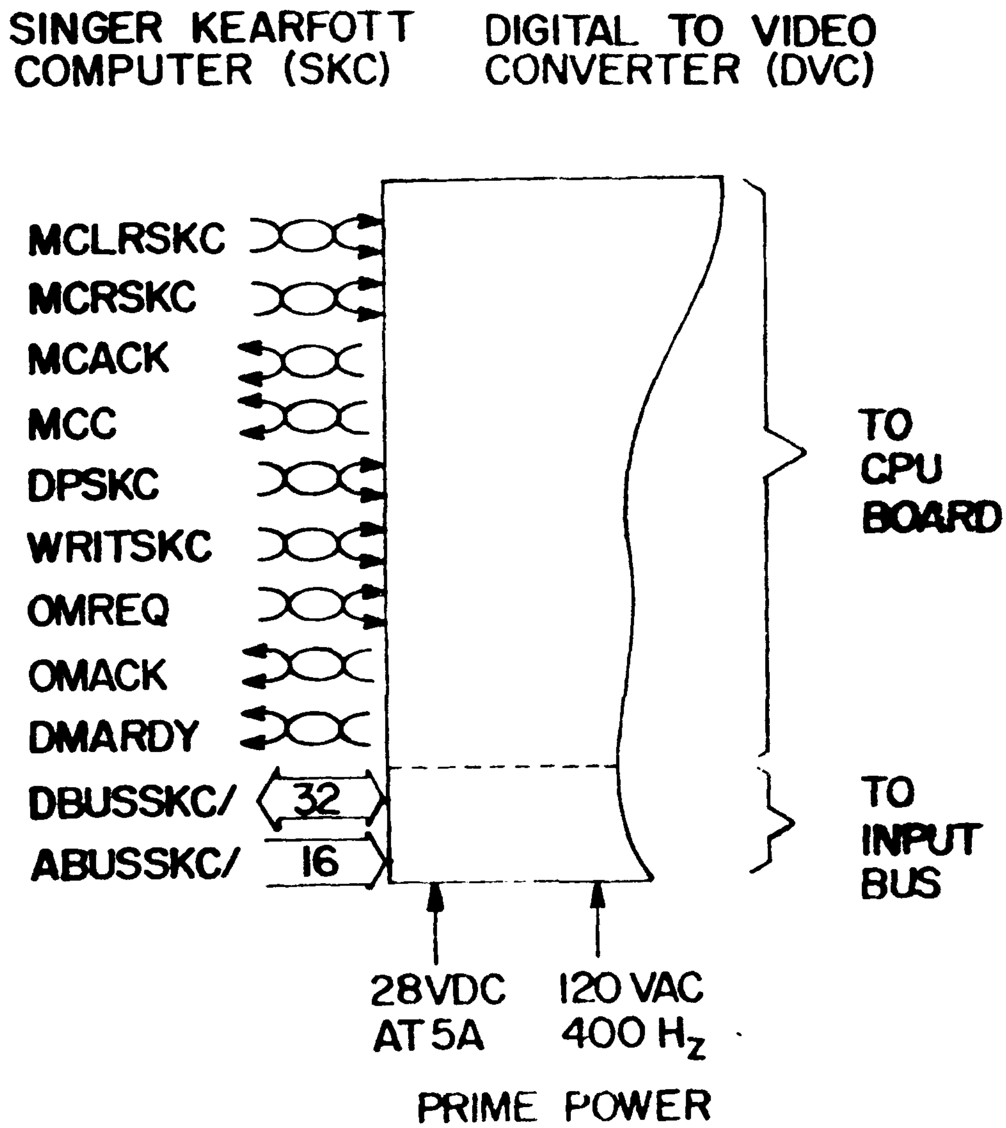


Figure 4. Singer Kearfott Computer - Digital to Video Converter Interface, for Operation with CPU.

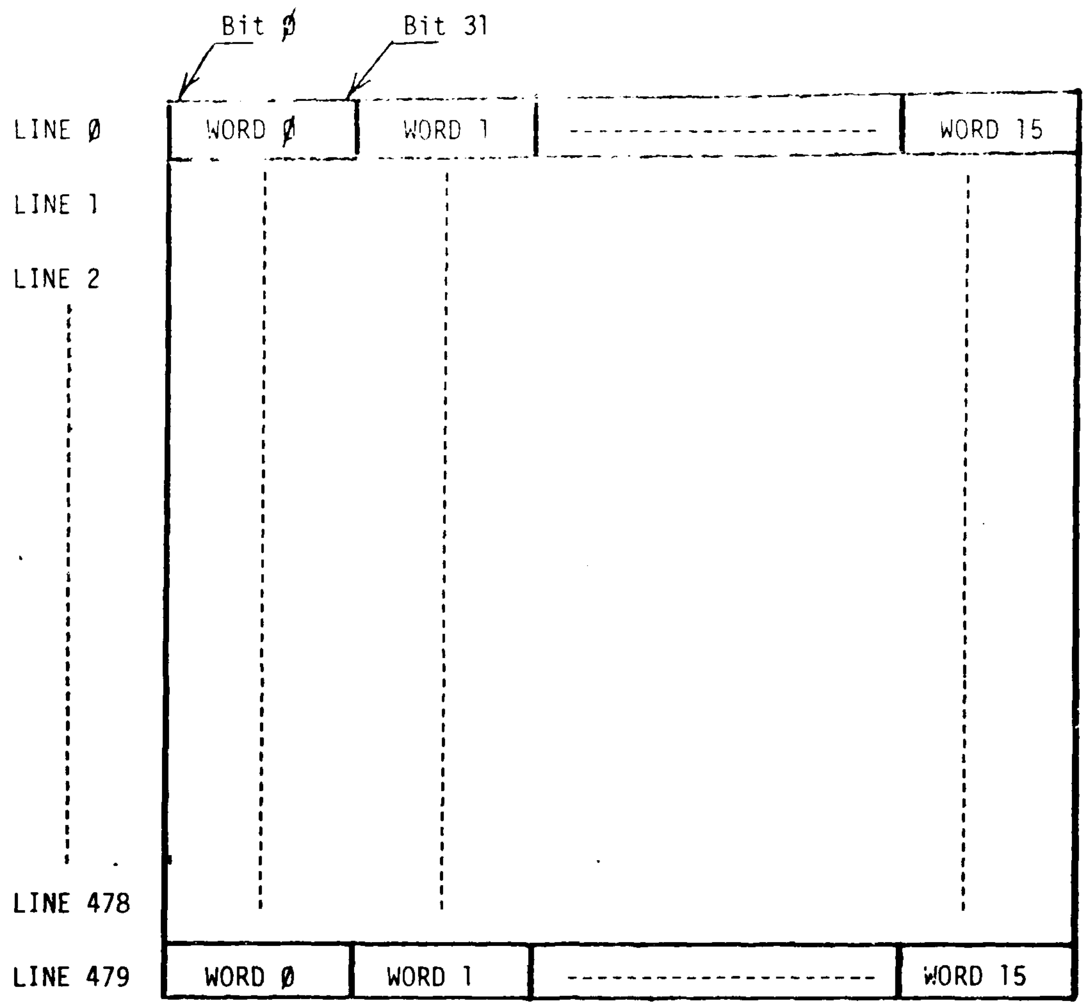


Figure 5. Map Display Format, 512 Pixels/Line Resolution

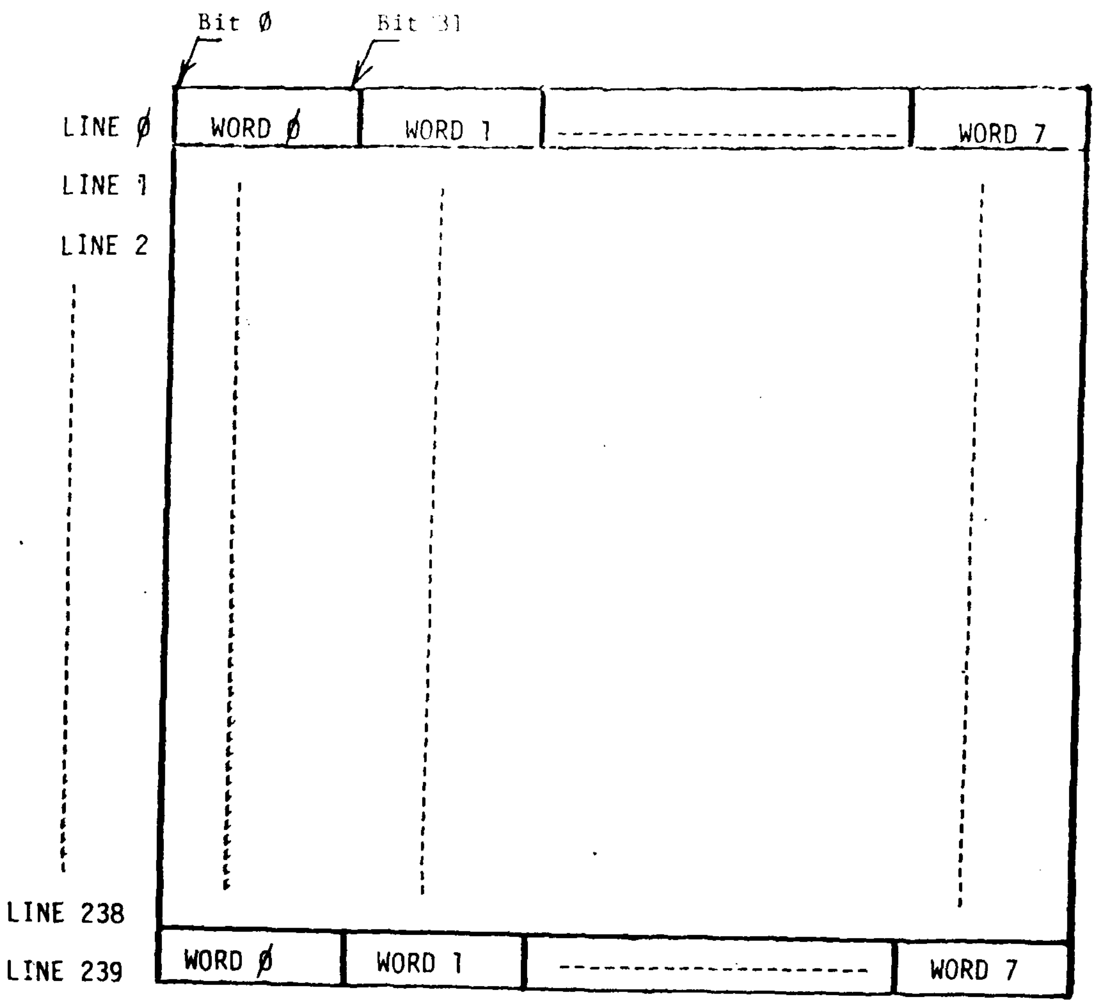


Figure 6. Map Display Format, 256 Pixels/Line Resolution

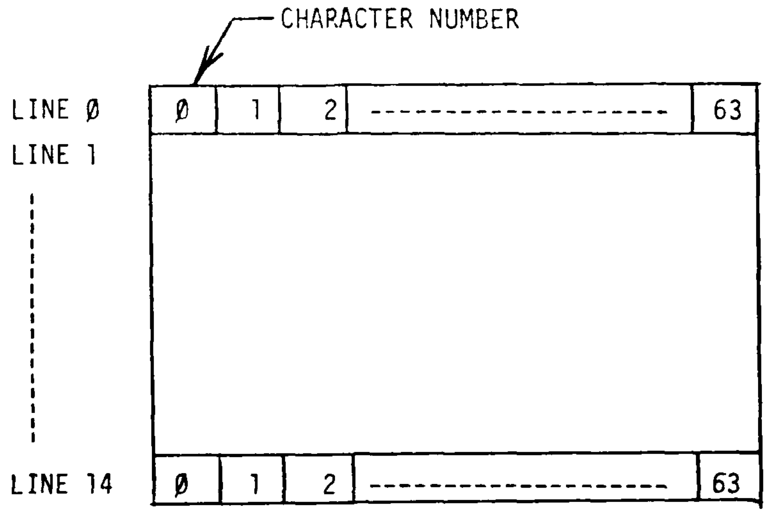


Figure 7. Alphanumeric Page Display Format, 64 Characters/Line, 15 Lines

BYTE NO.	BYTE 3								BYTE 2								BYTE 1								BYTE Ø							
	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø
WORD BIT NO.	31	3Ø	29	28	27	26	25	24	23	22	21	2Ø	19	18	17	16	15	14	13	12	11	1Ø	9	8	7	6	5	4	3	2	1	Ø
	HIGHEST ORDER CHARACTER																								LOWEST ORDER CHARACTER							

Figure 8. Alphanumeric Message Data Word Format as Stored in Display Memory

```
DATA BUS BIT NO                         7 6 5 4   3 2 1 0
   (1 BYTE)

CHARACTER GENERATOR                     S A6 . .   . . . A0
   ROM ADDRESS
```

DATA BIT 7 (S) is ROM SELECT CODE

0 = MC 6571 AL SHIFTED ASCII CHARACTERS AND GREEK

1 = MC 6574 L MATH SYMBOLS AND PICTURES

Figure 9. Alphanumeric Character Data Format

```
                |<- 8 DOTS ->|
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
    16 LINES    b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b x x x x x x x
                b b b b b b b b
                b b b b b b b b
```

b = BLANK

x = DOT LOCATION

Figure 10. Alphanumeric Character Dot Matrix Display Format

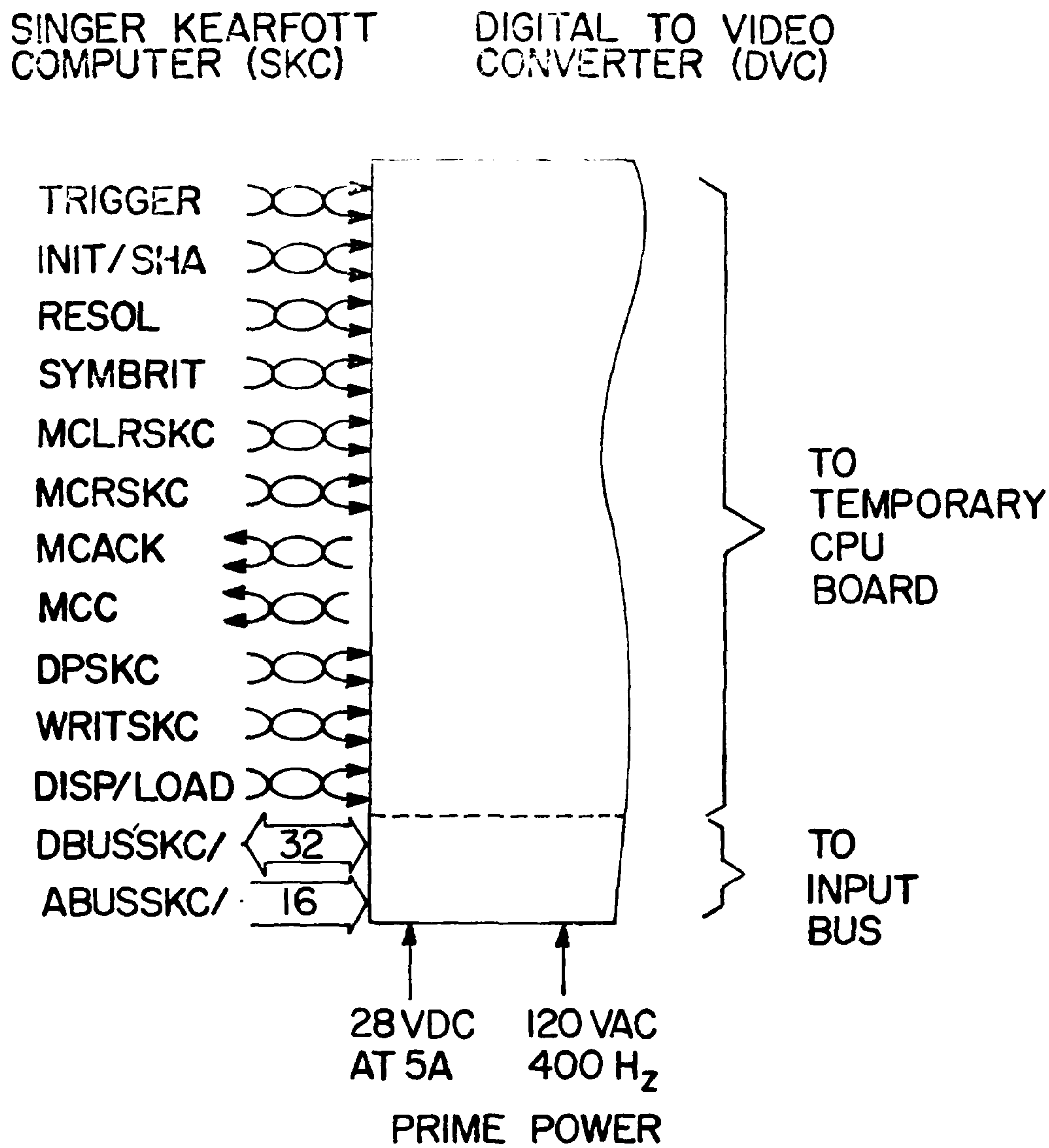


Figure A1. Singer Kearfott Computer - Digital to Video Converter Interface, for Operation with Temporary CPU.

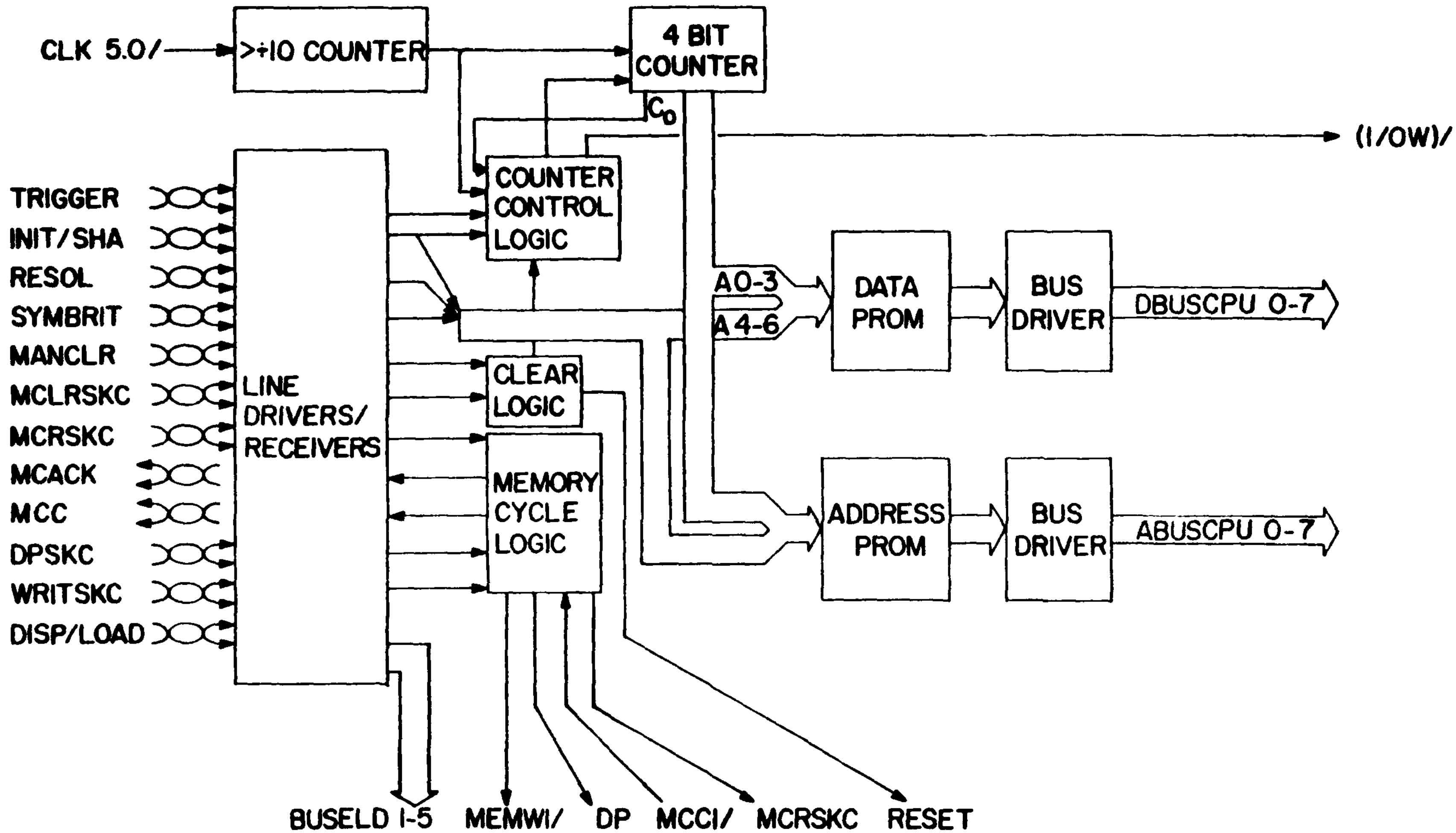


Figure A2. Temporary CPU Block Diagram

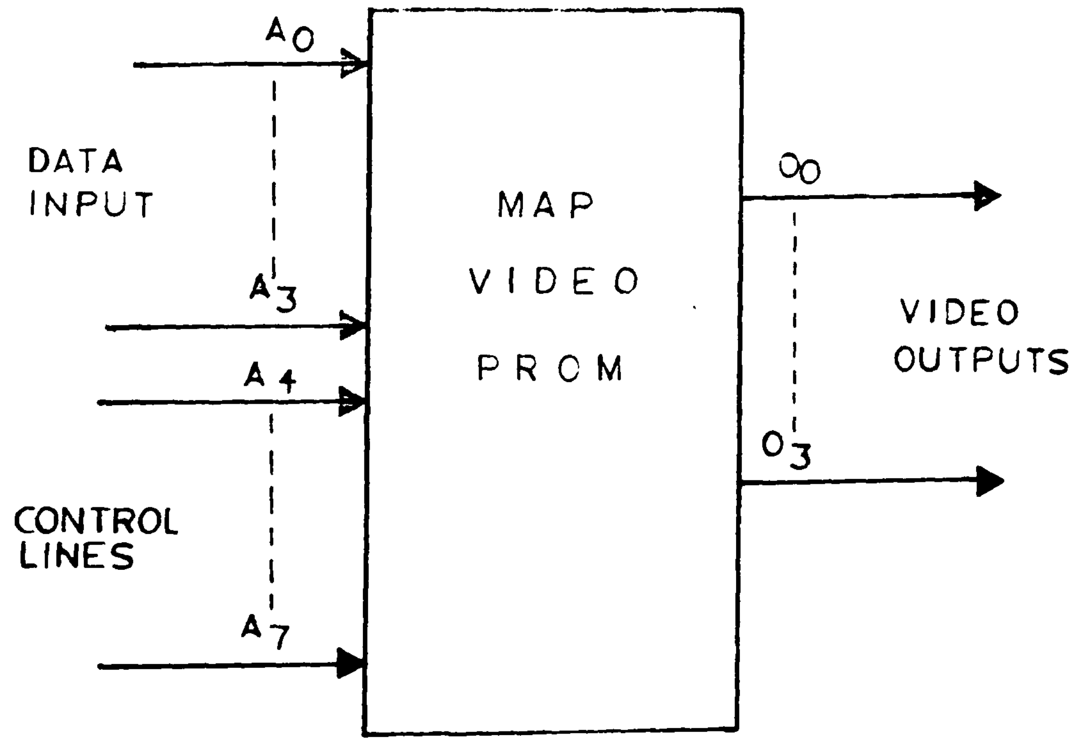


Figure B.. Map Video PROM Block Diagram

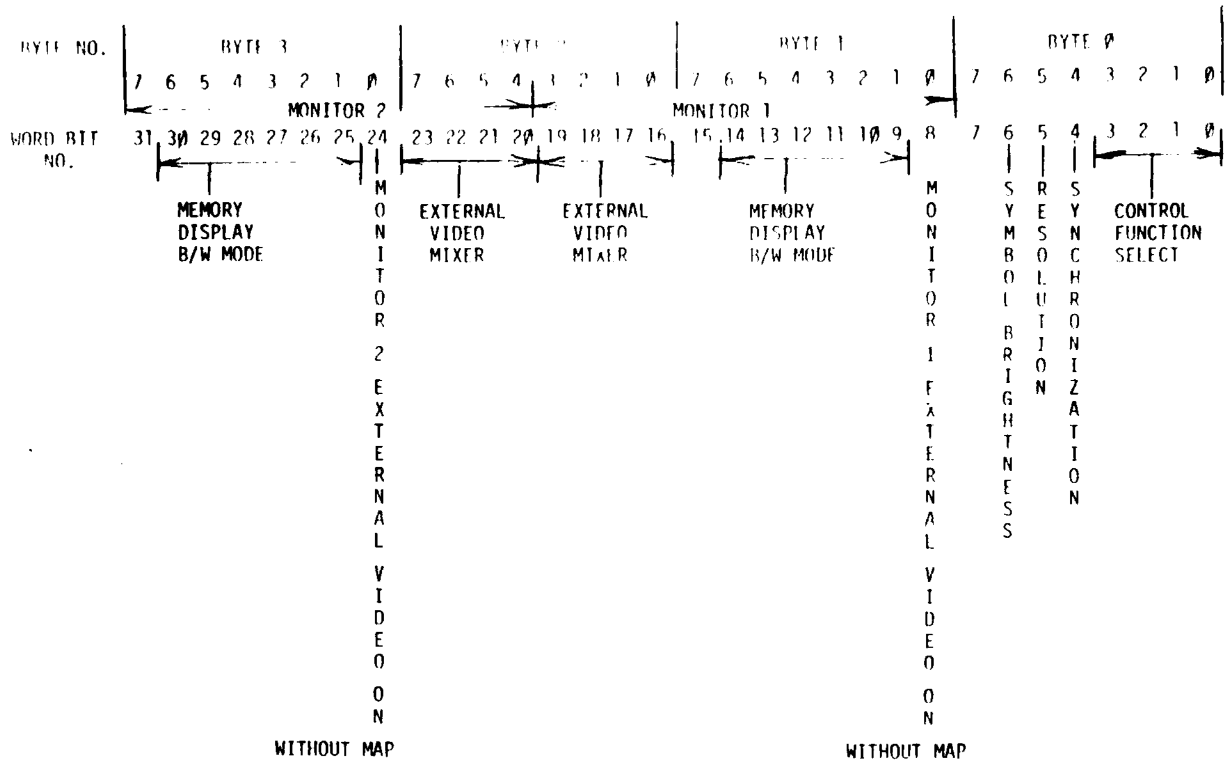


Figure C1. Control Word 0, Display

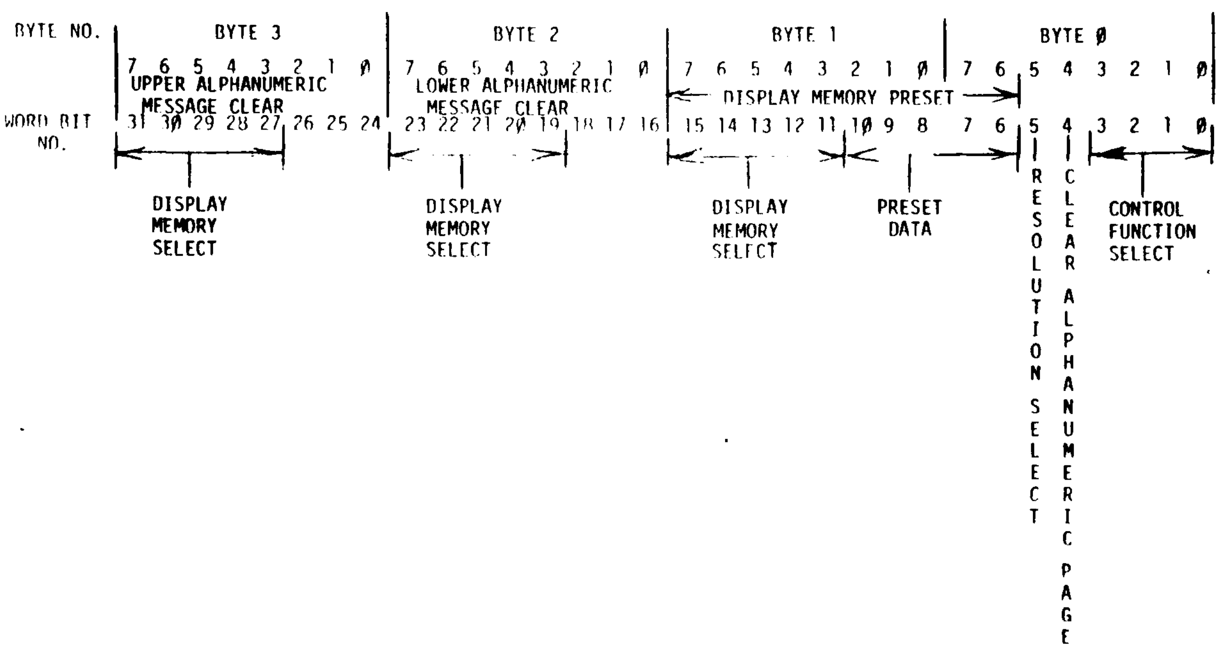


Figure C2. Control Word 1, Display

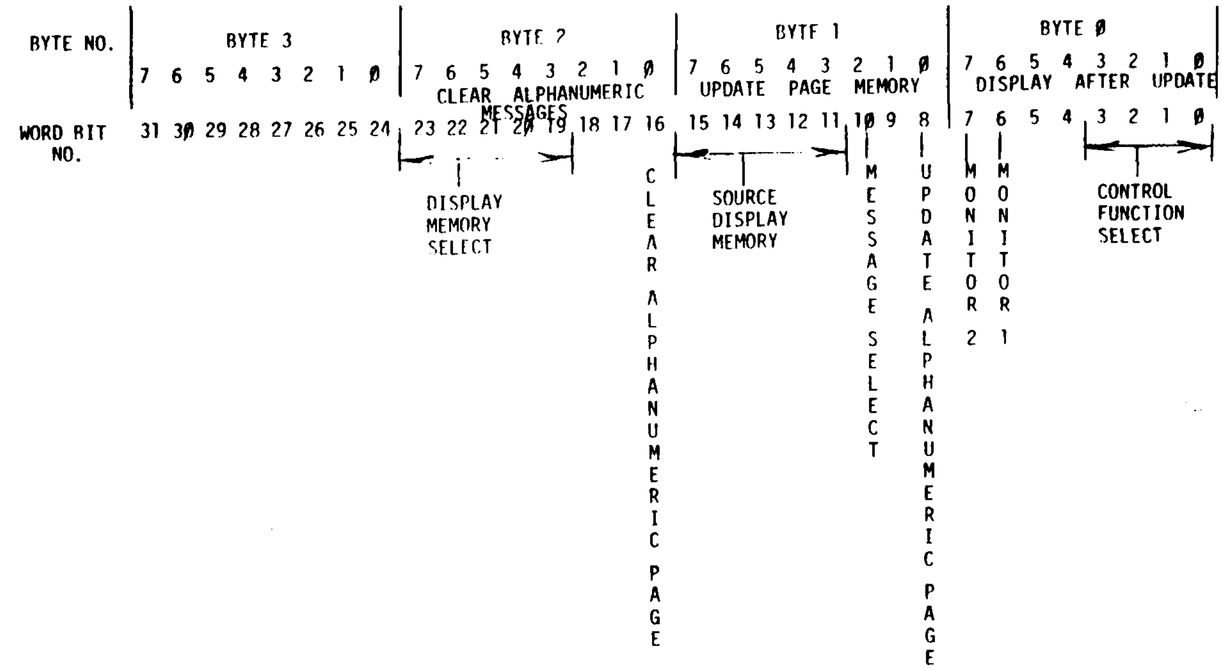


Figure C3. Control Word 2, Memory Preset/Clear

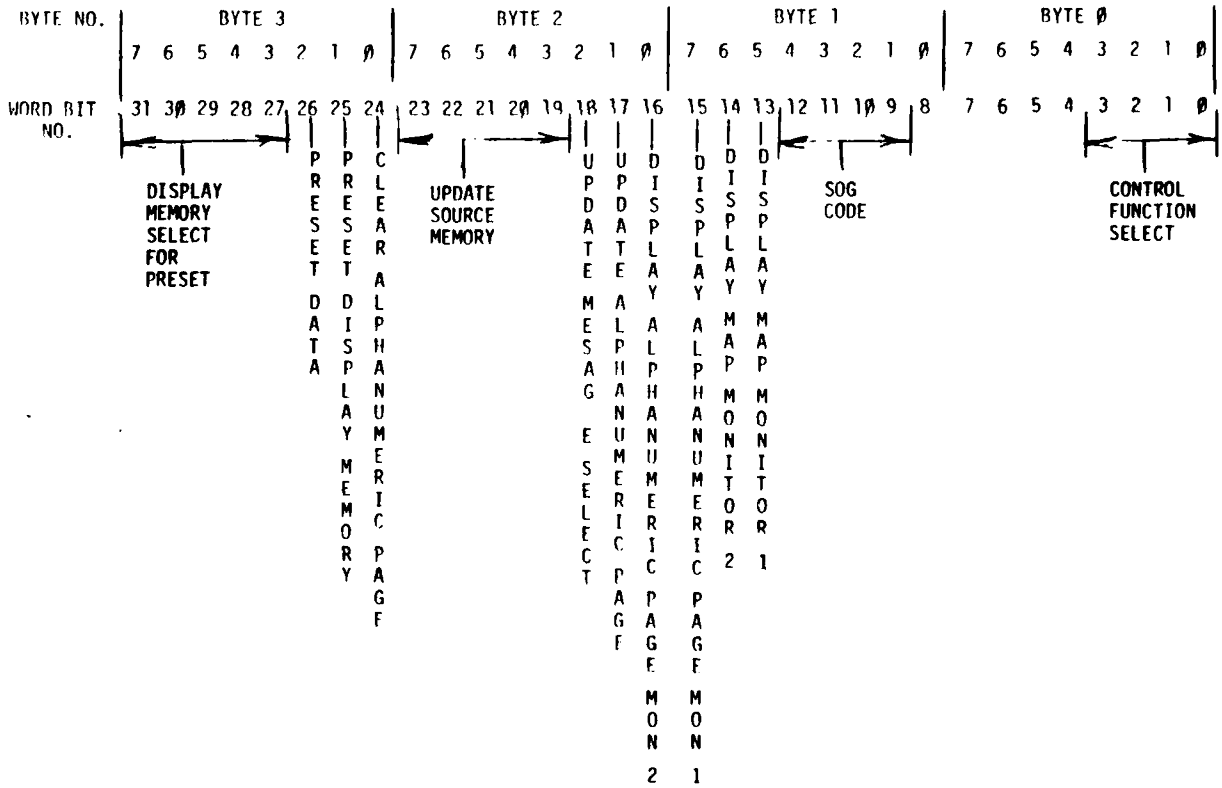


Figure C4. Control Word 3, Modify Alphanumeric Data

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